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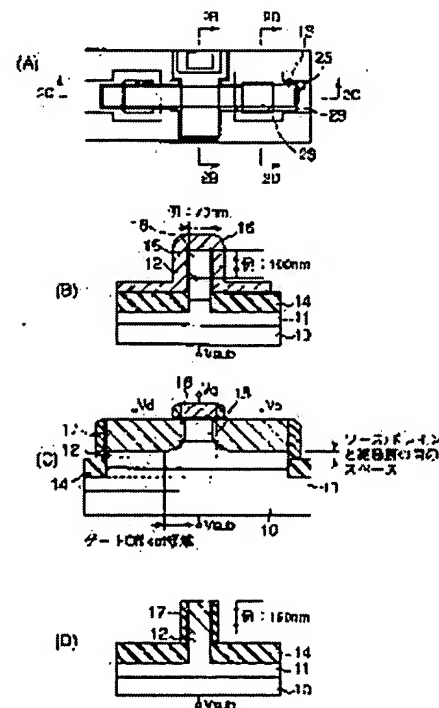
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(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which has a structure capable of contriving an increase in the performance of the device and uses at least each one part of the side surfaces of projected semiconductor layers as a channel region.

SOLUTION: A semiconductor device is provided with projected semiconductor layers 13, source and drain regions 17 and 17 provided in the layers 13, and a gate electrode 16 which has a sidewall gate part provided in a state that the sidewall gate is insulated from these layers 13 on the side surfaces of the layers 13 and gives a field effect to a channel region between the regions 17 and 17 via at least the side surfaces of the layers 13. The distance between the regions 17 and 17 is changed on the side surfaces of the layers 13.



## LEGAL STATUS

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CLAIMS

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## [Claim(s)]

[Claim 1] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, The semiconductor device with which it provides and distance between said source fields and said drain fields is characterized by changing in two side faces in which it faces mutually [ said convex semi-conductor layer ].

[Claim 2] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and the side-attachment-wall insulator layer prepared on the side face of said gate electrode, and the side face of said convex semi-conductor layer.

[Claim 3] The convex semi-conductor layer prepared on the substrate, and the isolation insulator layer formed in the perimeter of the lower field of said convex semi-conductor layer, The source field and drain field which were prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to said channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing, for the location of the top face of said isolation insulator layer being lower than the top face of said convex semi-conductor layer, and for the location of the deepest part of said source field and a drain field being the same as the location of the top face of said component demarcation membrane, or being lower than it.

[Claim 4] Said source field and a drain field are a semiconductor device according to claim 3 characterized by overlapping to said side-attachment-wall gate section.

[Claim 5] The 1st convex semi-conductor layer which was prepared on the substrate and was electrically connected with this substrate, Said 1st convex semi-conductor layer which was prepared on said substrate and was electrically connected with this substrate, and the 2nd convex semi-conductor layer with the same width of face, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, On the 1st side face of said 1st convex semi-conductor layer, and each 2nd side face of said 2nd convex semi-conductor layer in which this 1st side face was faced It has the side-attachment-wall gate section prepared in the condition of having insulated with these 1st and 2nd convex semi-conductor layer. Said 1st side face and said 2nd side face are minded at least. The semiconductor device characterized by providing the gate electrode which gives the electric field effect to the 1st channel field between said 1st source fields and said 1st drain fields, and the 2nd channel field between said 2nd source fields and said 2nd drain fields.

[Claim 6] The 1st convex semi-conductor layer which was prepared on the substrate and was electrically connected with this substrate, The 2nd convex semi-conductor layer which was prepared on said substrate and was electrically connected with this substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the

electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, The 1st wiring which connects mutually said 1st source field and said 2nd source field, The semiconductor device characterized by providing the 3rd wiring which connects the 2nd wiring which connects mutually said 1st drain field and said 2nd drain field, and said 1st gate electrode and said 2nd gate electrode of each other.

[Claim 7] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The source field and drain field which were prepared in said 1st convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer, And it has the gate contact section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the top face of said 2nd convex semi-conductor layer, respectively. The semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer.

[Claim 8] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. The electric conduction object which possesses the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and constitutes said side-attachment-wall gate section is a semiconductor device characterized by differing from the electric conduction object which constitutes said top-face gate section.

[Claim 9] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. The semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and wiring electrically contacted by said gate electrode by the top-face upper part of said convex semi-conductor layer.

[Claim 10] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, On the 1st side face of said 1st convex semi-conductor layer, and each 2nd side face of said 2nd convex semi-conductor layer in which this 1st side face was faced It has the side-attachment-wall gate section prepared in the condition of having insulated with these 1st and 2nd convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source fields and said 1st drain fields, and the 2nd channel field between said 2nd source fields and said 2nd drain fields through said 1st side face and said 2nd side face, The semiconductor device characterized by providing at least one 3rd convex semi-conductor layer of said 1st and 2nd source fields and said 1st and 2nd drain fields which connects either mutually at least.

[Claim 11] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field of the 1st conductivity type which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field of the 2nd conductivity type which were prepared in said 2nd convex semi-conductor layer, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, It is the semiconductor device characterized by providing and the depth of said 2nd source field and the 2nd drain field being deeper than the depth of said 1st source field and the 1st drain field.

[Claim 12] The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which estrange mutually, are prepared in said 2nd convex semi-conductor layer, and have the same conductivity type as said 1st source field and said 1st drain field, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, It is the semiconductor device characterized by providing and the depth of said 2nd source field and the 2nd drain field being deeper than the depth of said 1st source field and the 1st drain field.

[Claim 13] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing, constituting said gate electrode including the 1st layer and the 2nd layer at least, and said gate electrode constituting the word line of semiconductor memory equipment.

[Claim 14] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing, constituting said gate electrode including the 1st layer and the 2nd layer at least, and for said top face of the 1st layer being flat, and preparing said 2nd layer on said flat top face of the 1st layer.

[Claim 15] The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It is the semiconductor device characterized by providing and said gate electrode being constituted including the 1st layer and the 2nd layer at least, and for said top face of the 1st layer having a step, preparing said 2nd layer on a top face with said step of the 1st layer, and said top face of the 2nd layer being flat.

[Claim 16] The convex semi-conductor layer which is prepared on a substrate and has the 1st side face, the 2nd side face which countered this 1st side face, the 3rd side face in which it is located between the 1st and 2nd side face, the 4th side face which countered this 3rd side face, and a top face, The source field and drain field which are prepared in said convex semi-conductor layer, and contain the electric contact section, respectively, It has the side-attachment-wall gate section prepared on the 1st side face at least in the condition of said convex semi-conductor layer of having insulated with this convex semi-conductor layer. The gate electrode which gives the electric field effect to the channel field between the gate electrode aforementioned source field which gives the electric field effect at least to the channel field between said source fields and said drain fields through the 1st side face of said convex semi-conductor layer, and said drain field is provided. For said electric contact section, a part of 1st side face of said convex semi-conductor layer, a part of 2nd side face and a top face, and the 3rd and 4th side face are the semiconductor device characterized by straddling either a part respectively.

[Claim 17] The convex semi-conductor layer formed on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. It is the semiconductor device characterized by providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and the gate length of said side-attachment-wall gate section being shorter than the gate length of said top-face gate section.

[Claim 18] The process which etches a semi-conductor substrate and forms a convex semi-conductor layer in this semi-conductor substrate, The process which forms gate dielectric film on the side face of said convex semi-conductor layer at least, The process which forms the gate electrode which has the part which met the side face of said convex semi-conductor layer at least on said gate dielectric film, The process which forms a side-attachment-wall insulator layer on the side face of said gate electrode, and the side face of said convex semi-conductor layer, The manufacture approach of the semiconductor device characterized by providing the process which uses said gate electrode and said side-attachment-wall insulator layer for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer.

[Claim 19] The process which forms the insulator layer which has puncturing on a semi-conductor substrate, and the process which forms a convex semi-conductor layer on the semi-conductor substrate exposed from said puncturing, The process which forms gate dielectric film on the side face of said convex semi-conductor layer at least, The process which forms the gate electrode which has the part which met the side face of said convex semi-conductor layer at least on said gate dielectric film, The manufacture approach of the semiconductor device characterized by providing the process which uses said gate electrode for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer.

[Claim 20] Said convex semi-conductor layer is the manufacture approach of the semiconductor device according to claim 19 characterized by being formed by the epitaxial grown method.

[Claim 21] The process which forms a convex semi-conductor layer on a substrate, and the process which embeds the perimeter of said convex semi-conductor layer with an insulating material, The process which forms the slot for forming the side-attachment-wall gate section in said insulating material, The process which forms gate dielectric film on the side face of said convex semi-conductor layer exposed from said slot at least, The process which forms the gate electrode which has the side-attachment-wall gate section formed in said Mizouchi, The manufacture approach of the semiconductor device characterized by providing the process which uses said gate electrode for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer.

[Claim 22] Said side-attachment-wall gate section is a semiconductor device according to claim 1 characterized by having offset to a part of said source field and drain field.

[Claim 23] The semiconductor device according to claim 1 characterized by providing further a semi-conductor layer with high impurity concentration higher than said channel field prepared between said substrates and said source fields ranging over each between said substrates and said drain fields and between said substrates and said channel fields.

[Claim 24] It is the semiconductor device according to claim 1 characterized by providing the 1st gate dielectric film formed on the side face of said convex semi-conductor layer, and the 2nd gate dielectric film formed on the top face of said convex semi-conductor layer, and said 2nd gate dielectric film being thicker than said 1st gate dielectric film.

[Claim 25] Said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a forward tapered shape toward the top face of this convex semi-conductor layer from said substrate.

[Claim 26] The lower field of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a forward tapered shape toward the top face of this convex semi-conductor layer from said substrate.

[Claim 27] The configuration of the pars-basilaris-ossis-occipitalis corner of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a round configuration.

[Claim 28] The configuration of the up corner of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being a round configuration.

[Claim 29] The include angle of the up corner of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by exceeding 90 degrees.

[Claim 30] The semiconductor device according to claim 1 characterized by providing further the insulating material prepared between said substrate and said convex semi-conductor layer, and the semiconductor region of the same conductivity type as said channel field being in each between the pars basilaris ossis occipitalis of said source field, and said insulating material, and between the pars basilaris ossis occipitalis of said drain field, and said insulating material.

[Claim 31] Said convex semi-conductor layer is a semiconductor device according to claim 30 characterized by being an amorphous silicon.

[Claim 32] For said electric contact section, said source field and a drain field are a semiconductor device according to claim 1 characterized by straddling respectively a part of side face of said convex semi-conductor layer, a part of other side faces which countered this side face, and the top face of said convex semi-conductor layer including the electric contact section, respectively.

[Claim 33] It is the semiconductor device according to claim 1 characterized by providing the 2nd gate dielectric film formed on the top face of the 1st gate dielectric film formed on the side face of said convex semi-conductor layer, and said convex semi-conductor layer, and said 2nd gate dielectric film being thinner than said 1st gate dielectric film.

[Claim 34] It is the semiconductor device according to claim 1 which possesses the 1st gate dielectric film formed on the side face of said convex semi-conductor layer, and the 2nd gate dielectric film formed on the top face of said convex semi-conductor layer, and is characterized by the configuration of the up corner of said 1st gate dielectric film being a round configuration.

[Claim 35] The distance between said source fields and said drain fields is a semiconductor device according to claim 1 characterized by becoming long toward the lower part from the upper part of said convex semi-conductor layer.

[Claim 36] The high impurity concentration of said source field and the high impurity concentration of said drain field are a semiconductor device according to claim 1 characterized by becoming low toward the lower part from the upper part of said convex semi-conductor layer.

[Claim 37] Said side-attachment-wall gate section is a semiconductor device according to claim 1 characterized by being formed in the bottom of said source field and said drain field along two side faces in which it faces mutually [ said convex semi-conductor layer ].

[Claim 38] The width of face of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being smaller than 0.2 micrometers.

[Claim 39] The width of face of said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by being smaller than the depth of said source field, and the depth of said drain field.

[Claim 40] At least one of said source field and said the drain fields is a semiconductor device according to claim 1 characterized by including two kinds of diffusion layers of a high concentration diffusion layer with deep high impurity concentration, and a low concentration diffusion layer with high impurity concentration thinner than said high concentration diffusion layer at least.

[Claim 41] Said convex semi-conductor layer is a semiconductor device according to claim 1 characterized by connecting with said substrate electrically.

[Claim 42] Said substrate is a semiconductor device according to claim 1 characterized by being conductivity.

[Claim 43] It is the semiconductor device according to claim 1 which possesses further the gate dielectric film formed between each of two side faces in which said side-attachment-wall gate section is faced mutually [ said convex semi-conductor layer ], and is characterized by said gate dielectric film consisting of an oxide of Ta, Sr, aluminum, Si, Zr, Hf, La, and Ti which contains any one at least.

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[Translation done.]



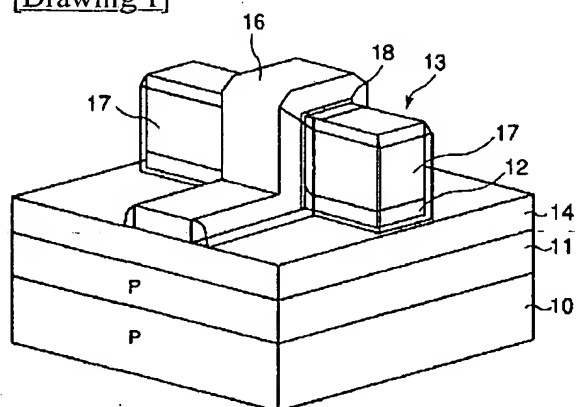
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## DRAWINGS

[Drawing 1]



[Drawing 2]

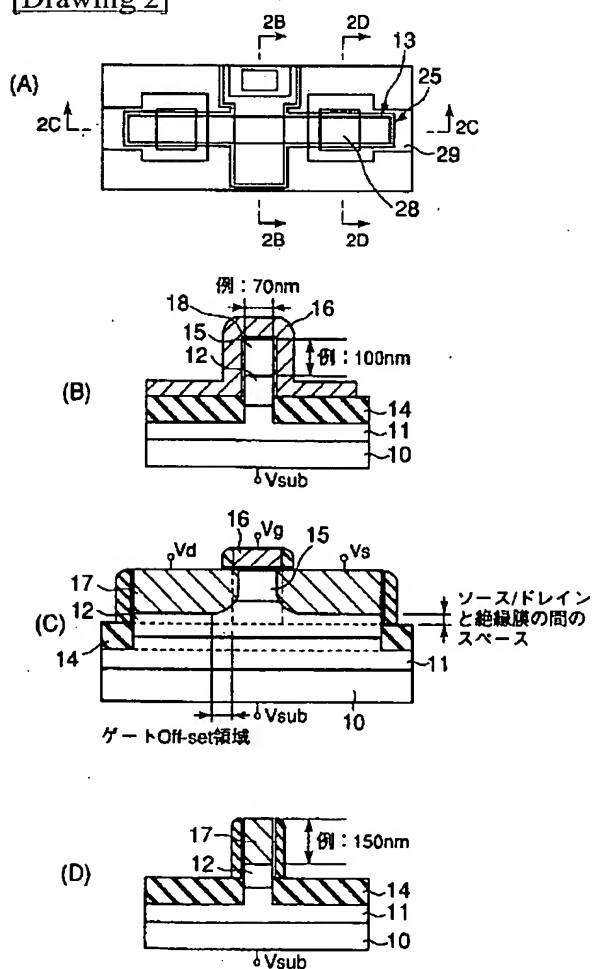
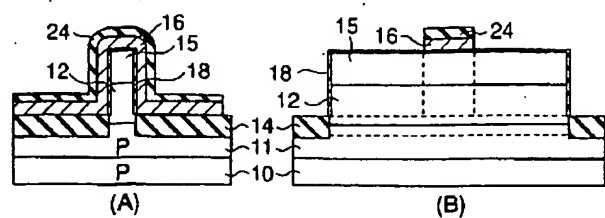


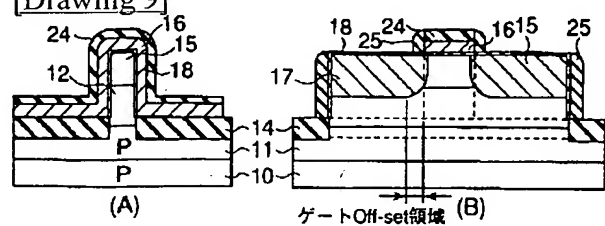


Fig. 1. Cross-sectional views of the device. (A) shows the initial state with a thin layer 15 on a substrate with layers 10, 11, and 14. A layer 12 is on top of 14. (B) shows the device after growth, with a thicker layer 15 and a new layer 18 on top of 12.

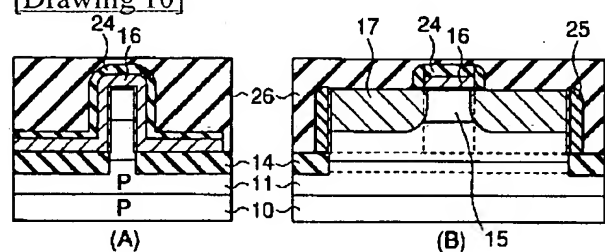
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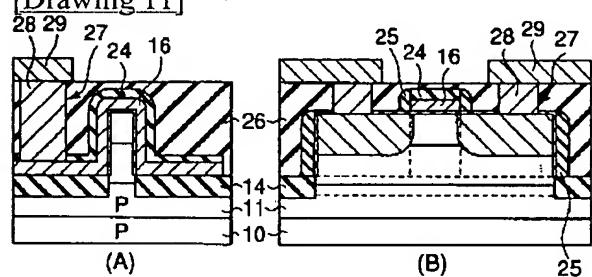
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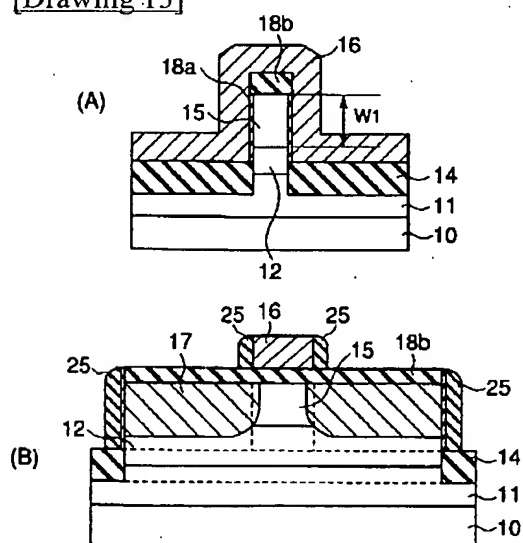
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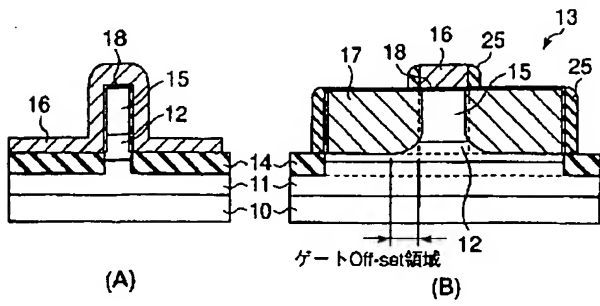
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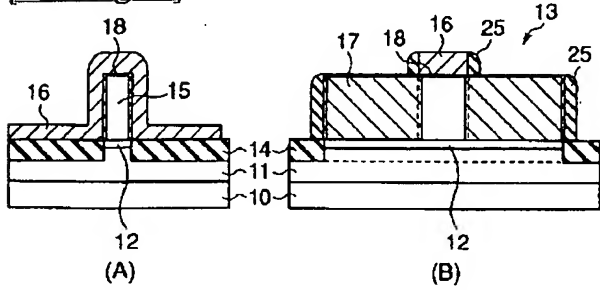
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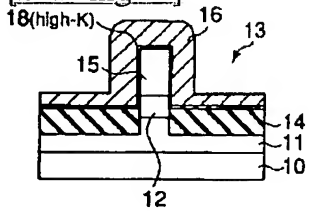
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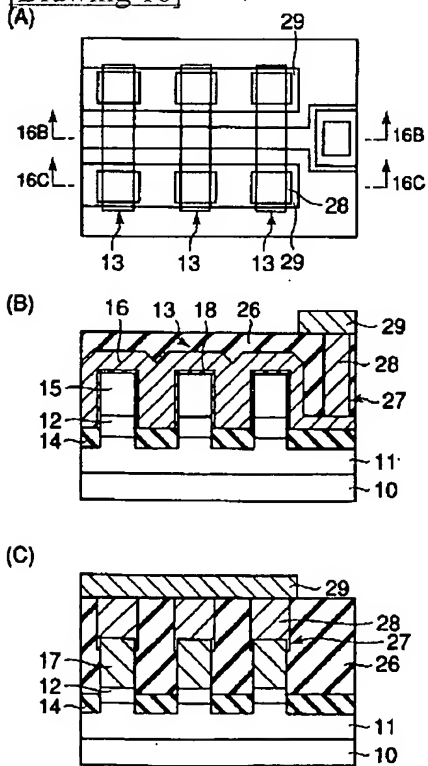
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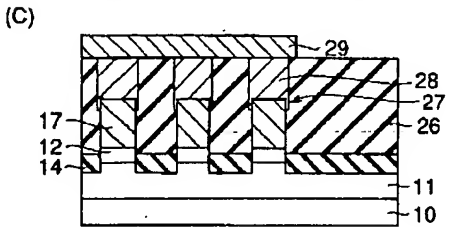
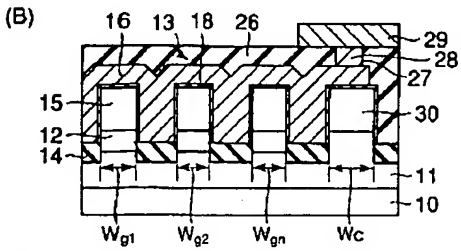
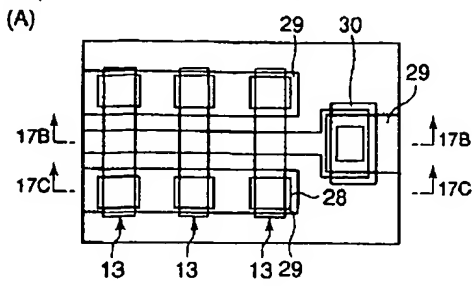
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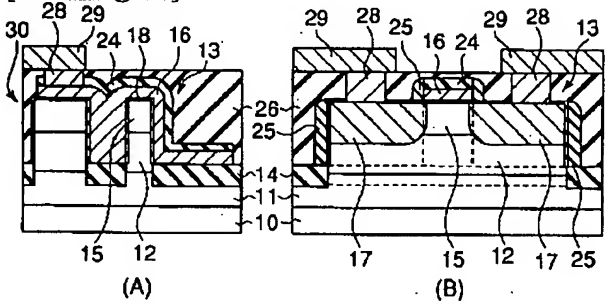
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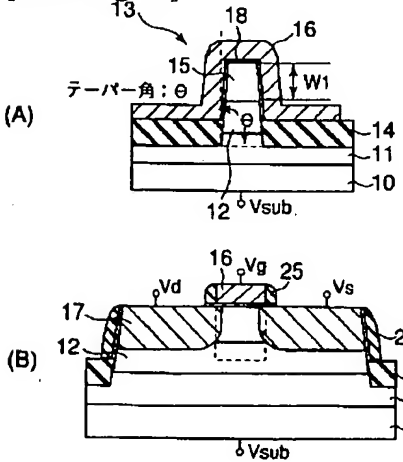
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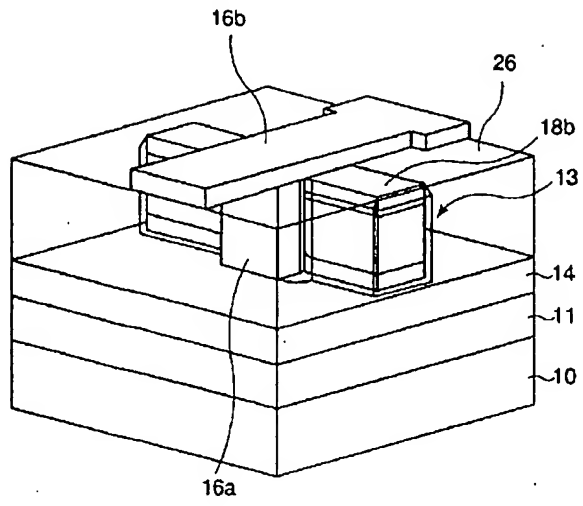
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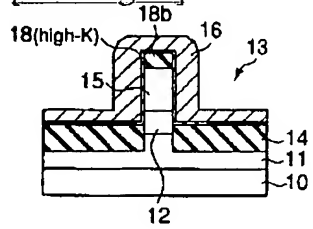
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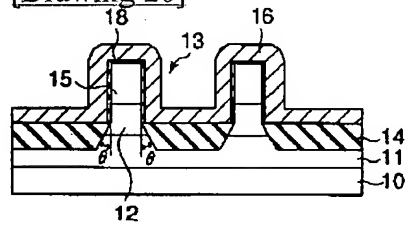
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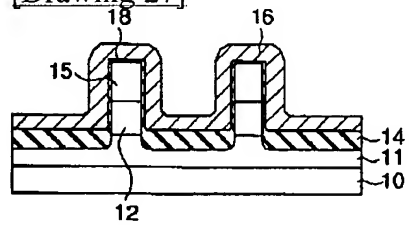
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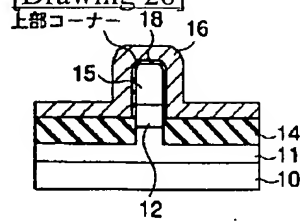
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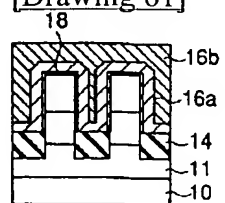
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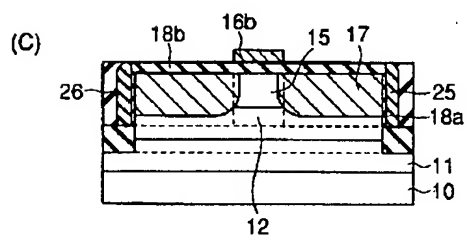
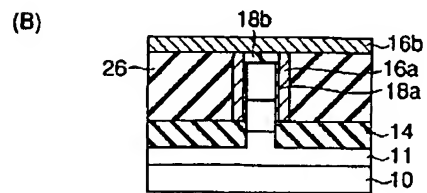
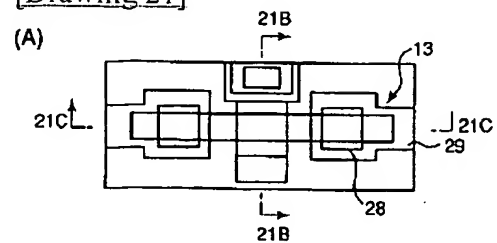
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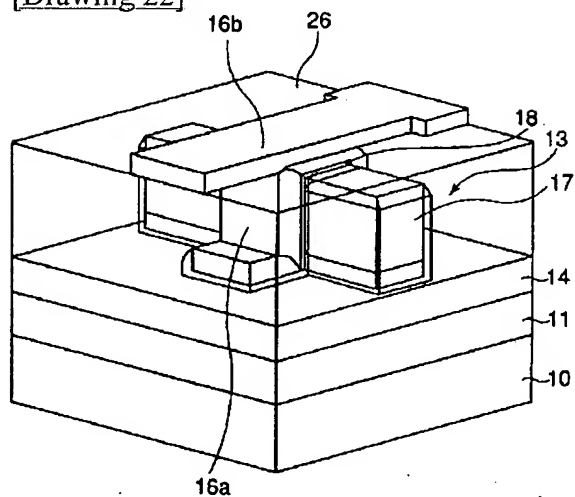
[Drawing 61]



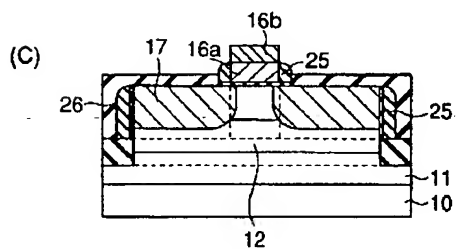
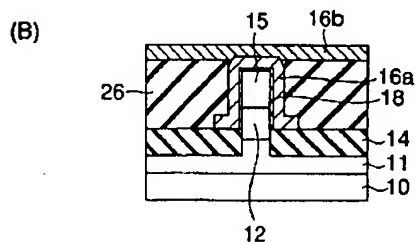
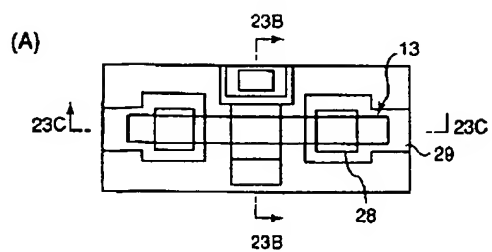
[Drawing 21]



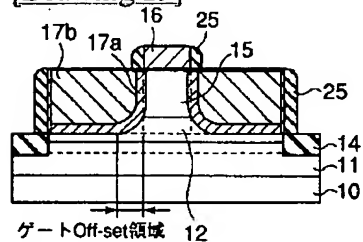
[Drawing 22]



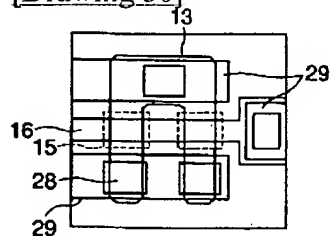
[Drawing 23]



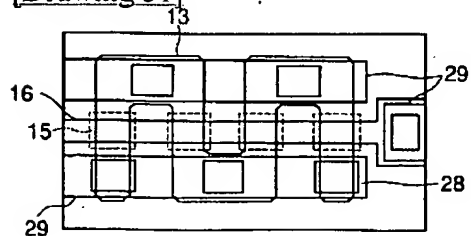
[Drawing 29]



[Drawing 30]

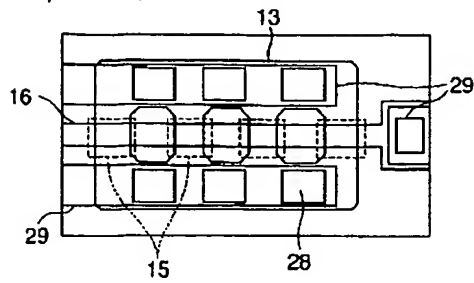


[Drawing 31]

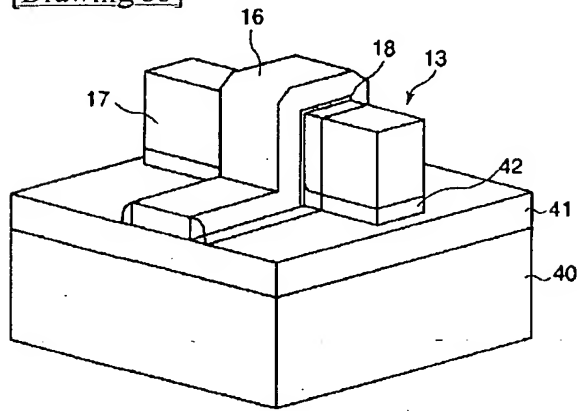


[Drawing 32]

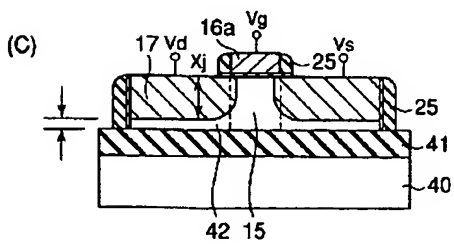
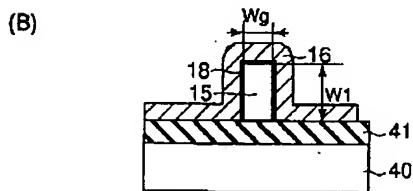
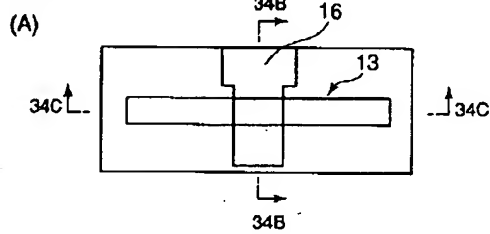




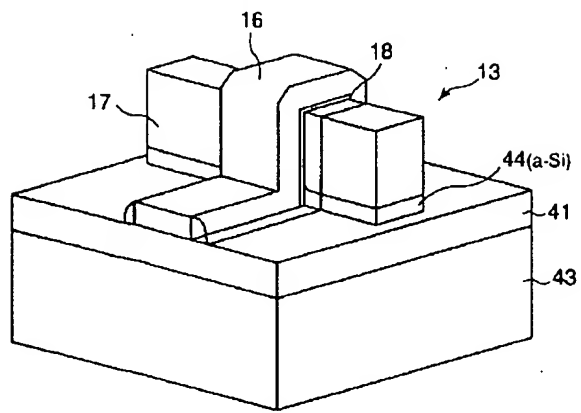
[Drawing 33]



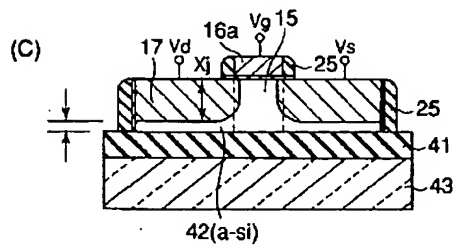
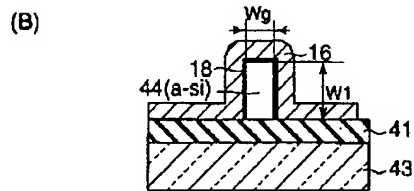
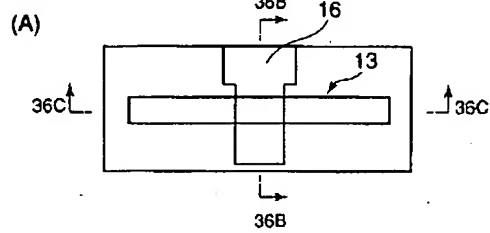
[Drawing 34]



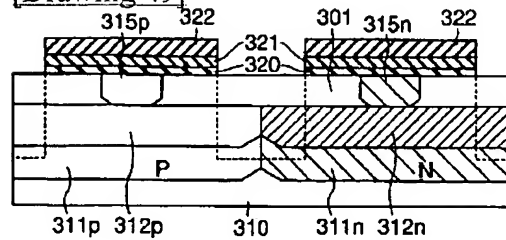
[Drawing 35]



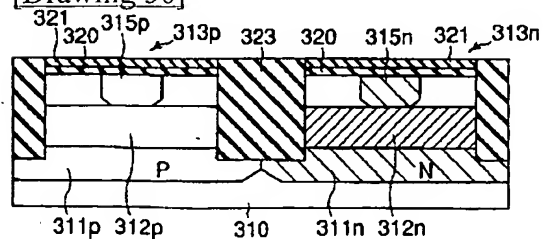
[Drawing 36]



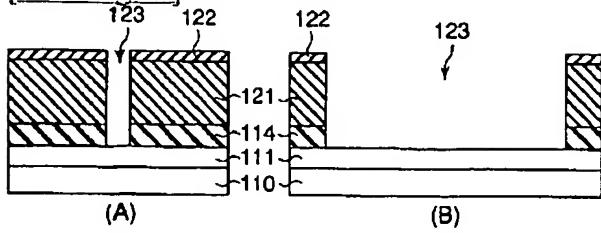
[Drawing 49]



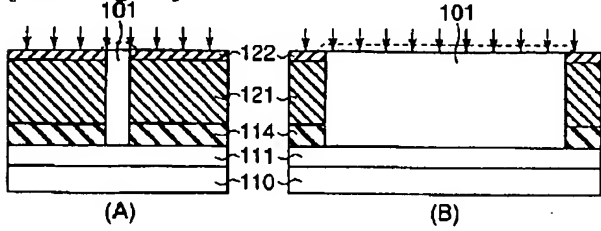
[Drawing 50]



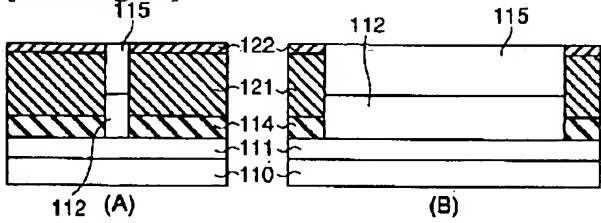
[Drawing 37]



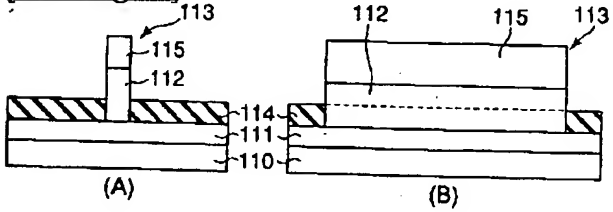
[Drawing 38]



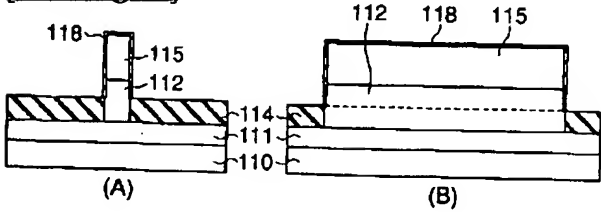
[Drawing 39]



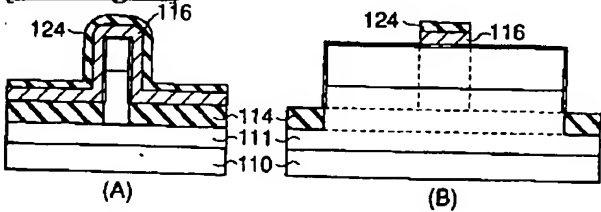
[Drawing 40]



[Drawing 41]

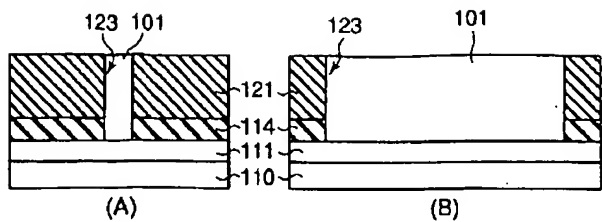


[Drawing 42]

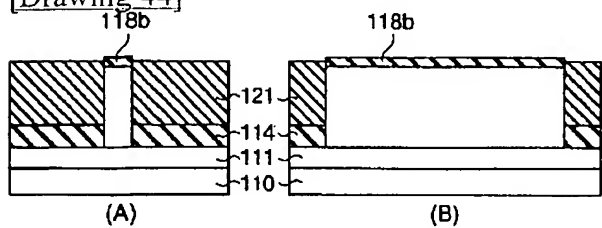


[Drawing 43]

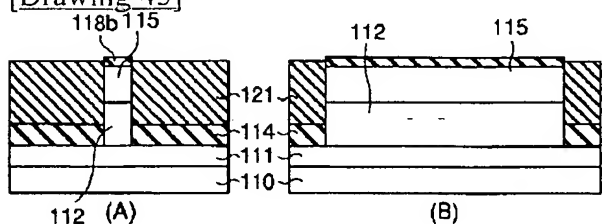




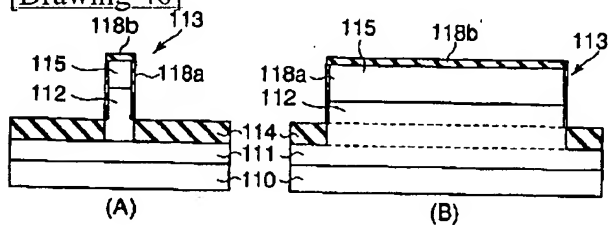
[Drawing 44]



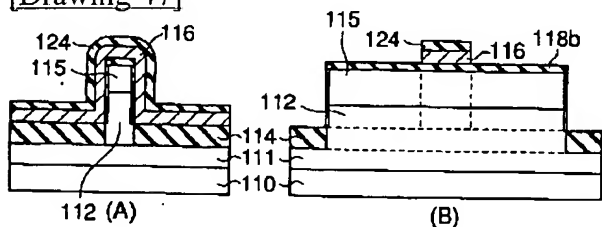
[Drawing 45]



[Drawing 46]



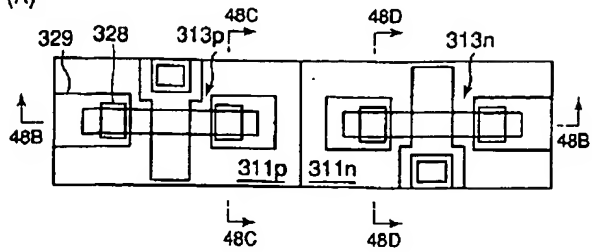
[Drawing 47]



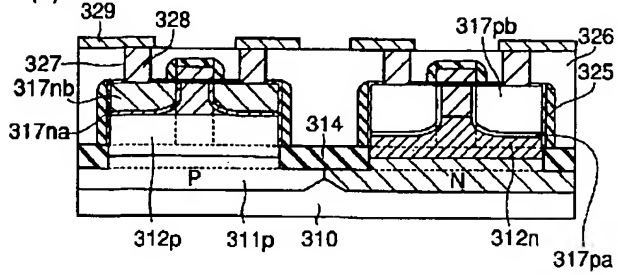
[Drawing 48]



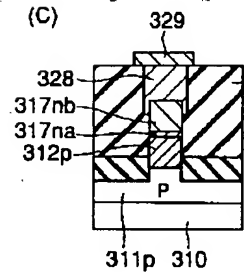
(A)



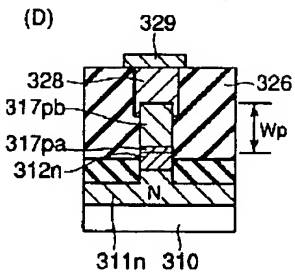
(B)



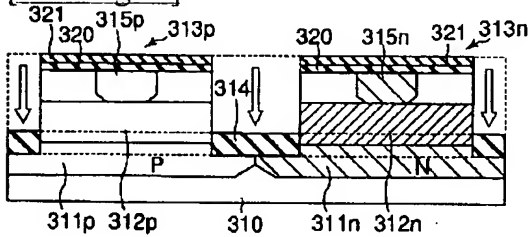
(C)



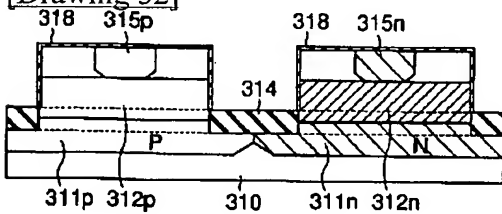
(D)



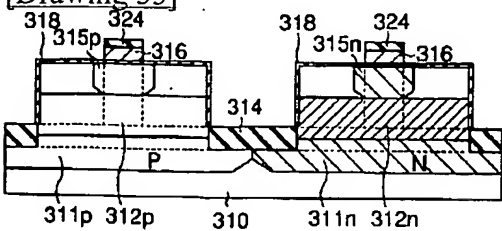
[Drawing 51]



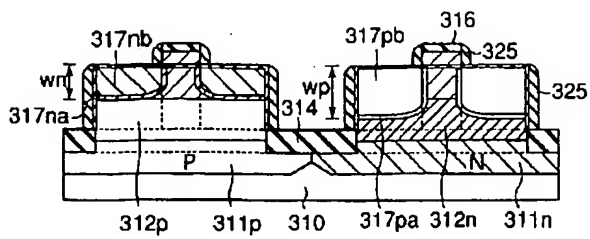
[Drawing 52]



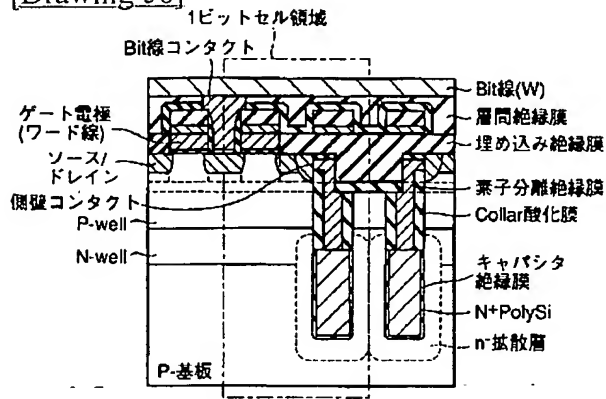
[Drawing 53]



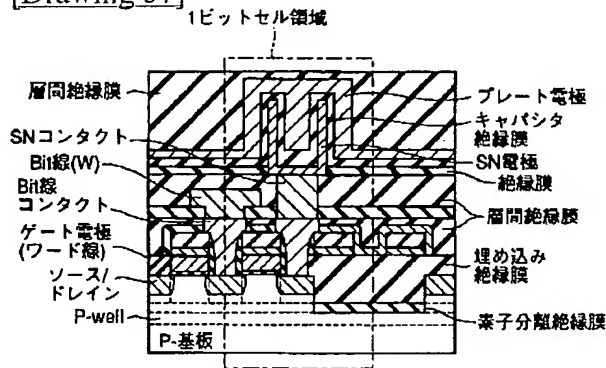
[Drawing 54]



[Drawing 56]

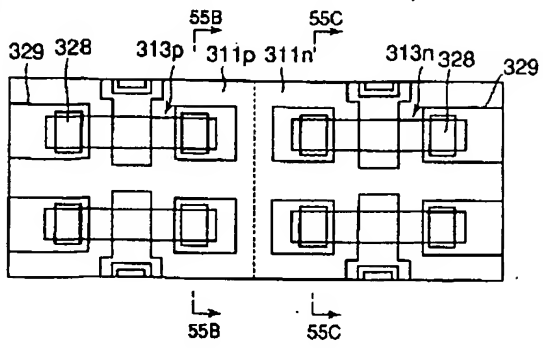


[Drawing 57]

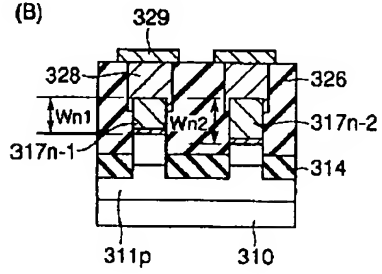


[Drawing 55]

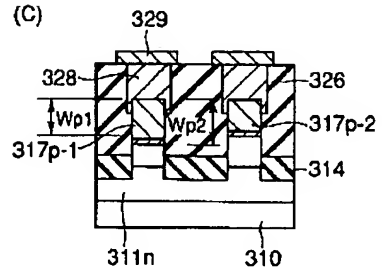
(A)



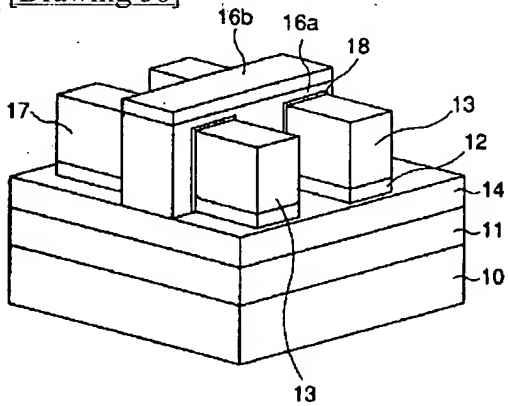
(B)



(C)

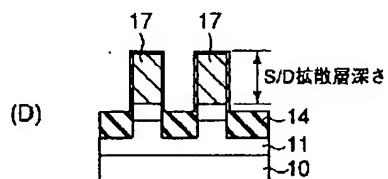
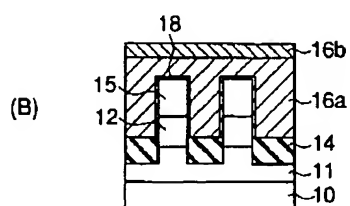


[Drawing 58]

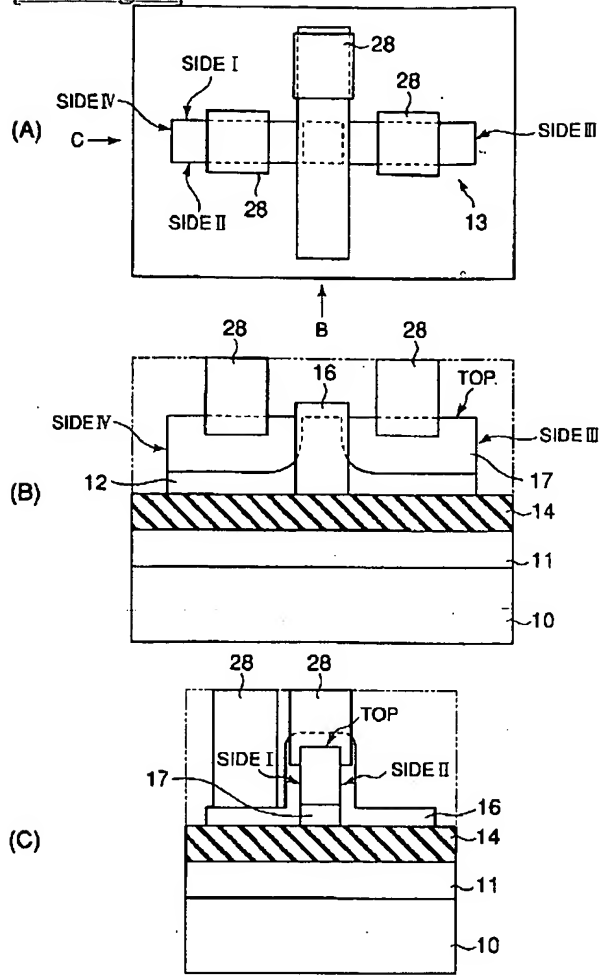


[Drawing 59]

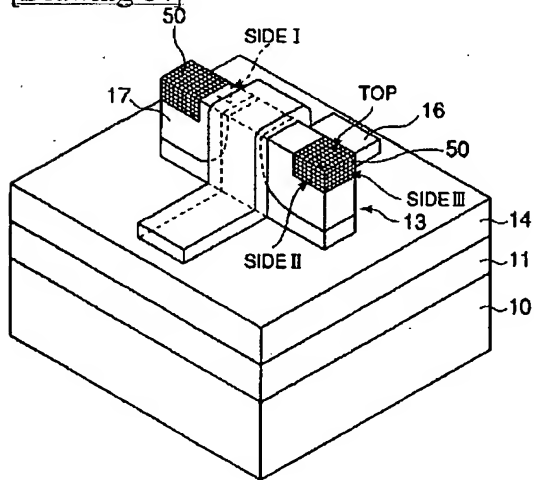




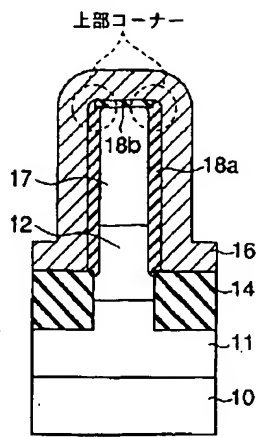
[Drawing 63]



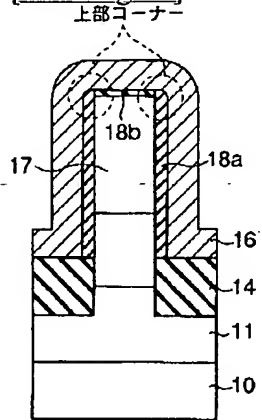
[Drawing 64]



[Drawing 66]

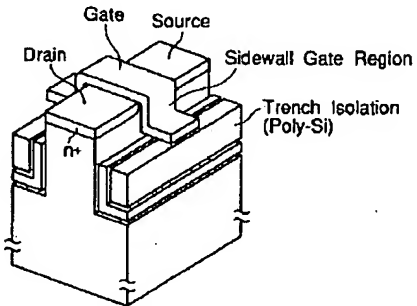


[Drawing 67]



[Drawing 79]

Trench Isolated (TIS) Transistor (1987 IEDM)

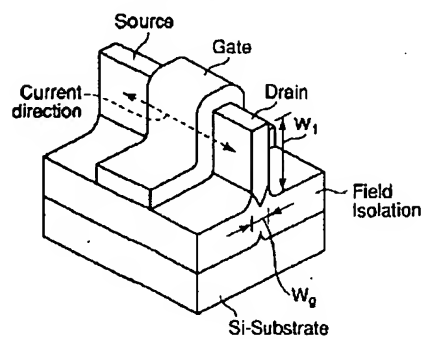


[Drawing 65]



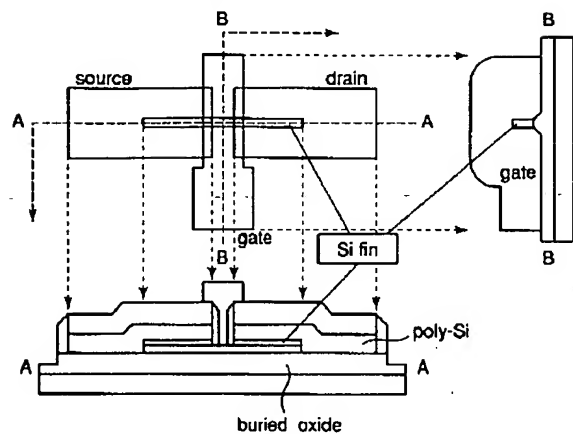
[http://www4.ipdl.ncipi.go.jp/cgi-bin/tran\\_web\\_cgi\\_ejje](http://www4.ipdl.ncipi.go.jp/cgi-bin/tran_web_cgi_ejje)

DELTA構造 (1989 IEDM)

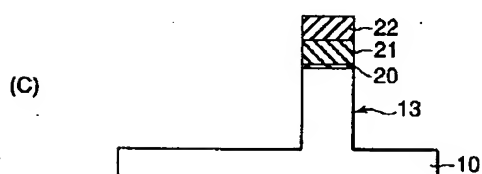
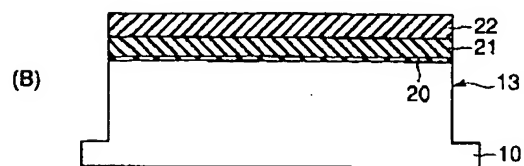
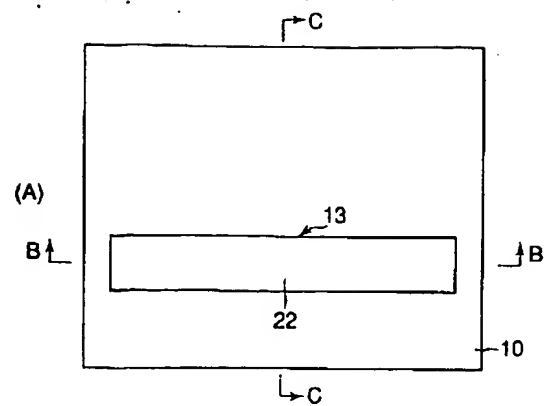


[Drawing 81]

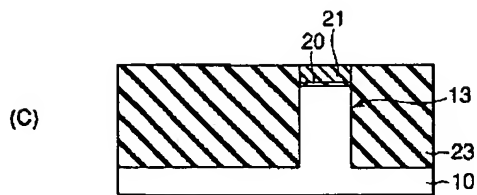
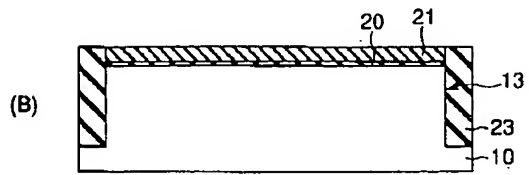
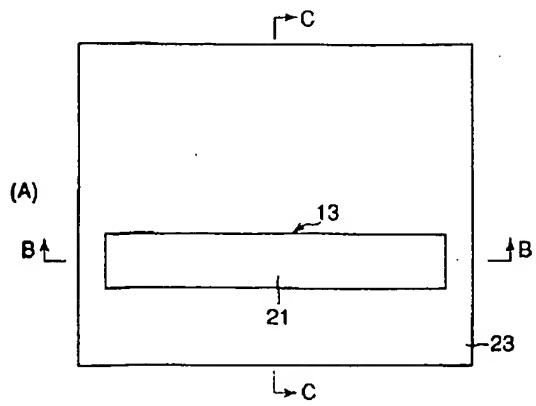
Folded-channel MOSFET (1998 IEDM)



[Drawing 69]

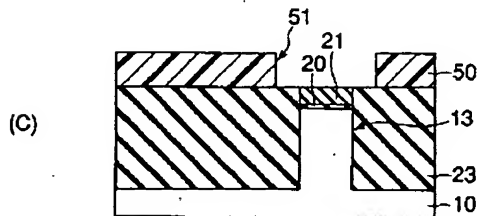
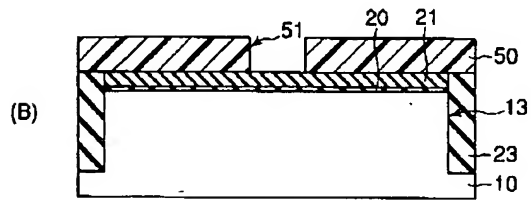
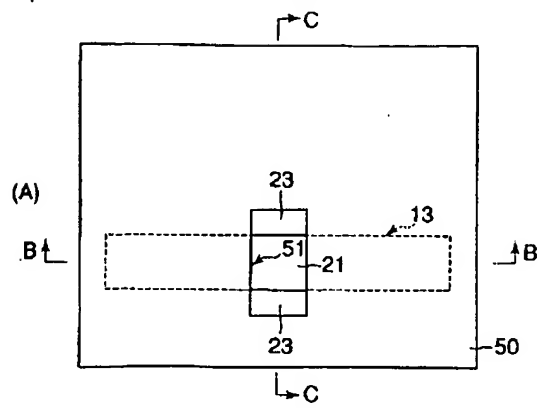


[Drawing 70]

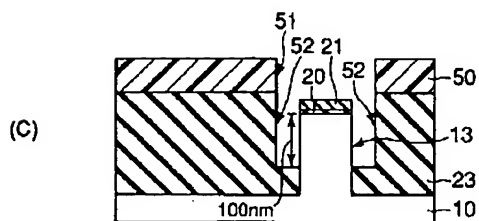
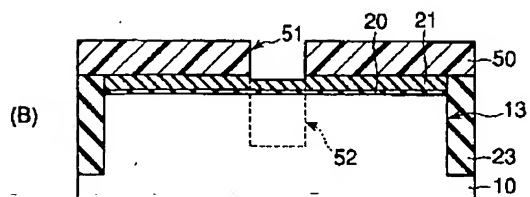
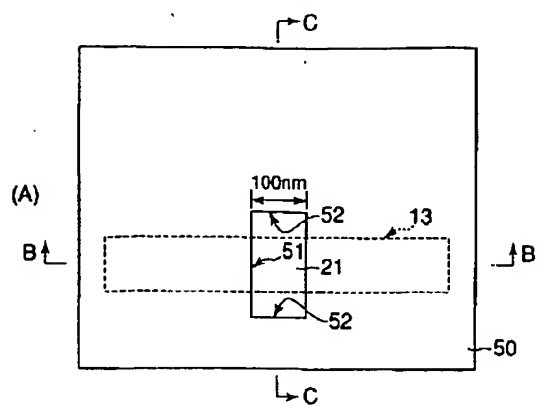


[Drawing 71]

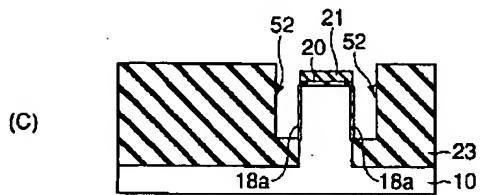
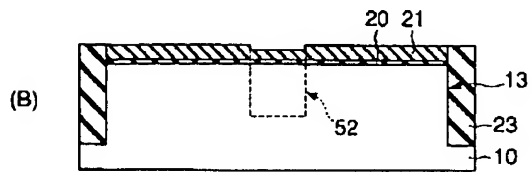
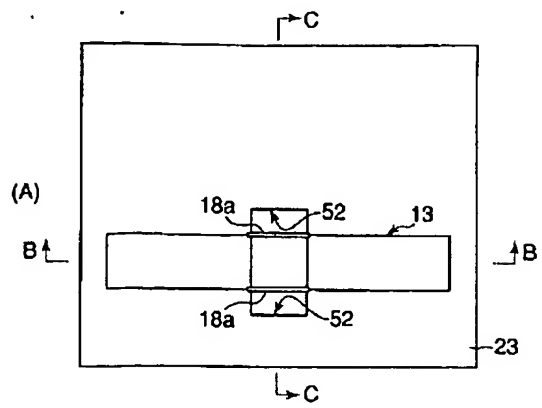




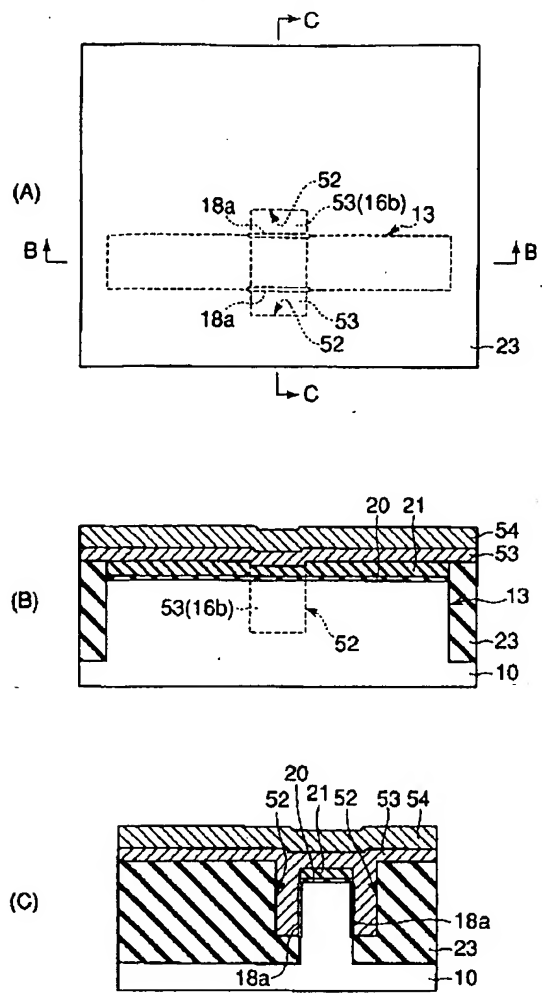
[Drawing 72]



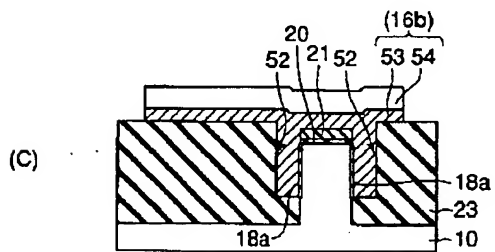
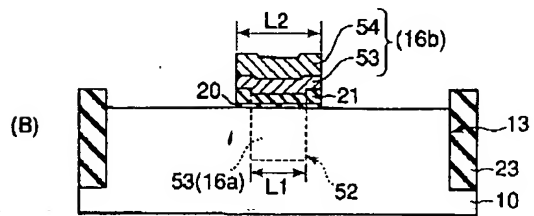
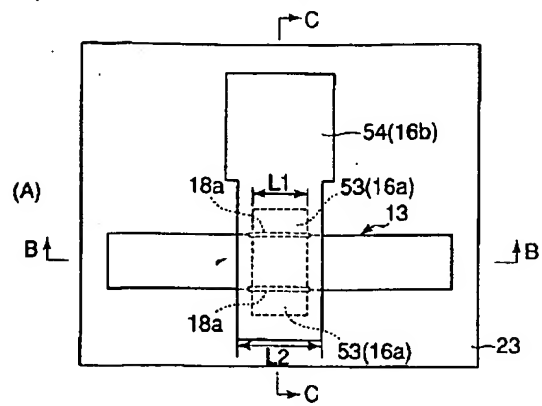
[Drawing 73]



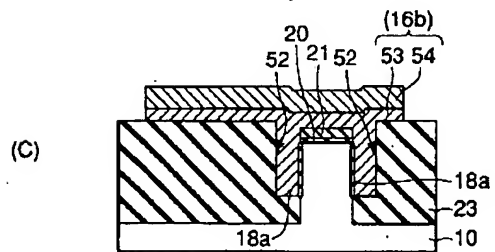
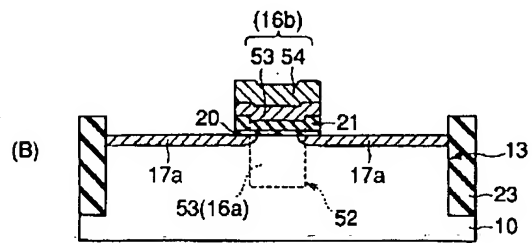
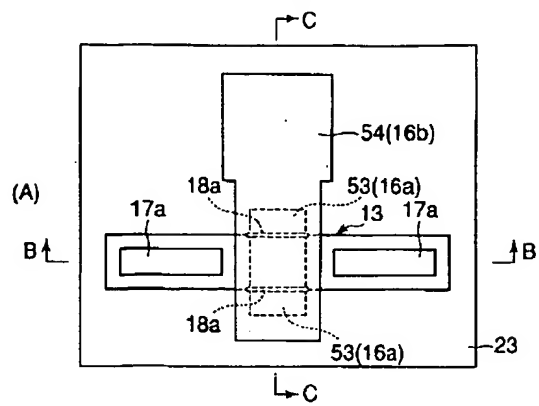
[Drawing 74]



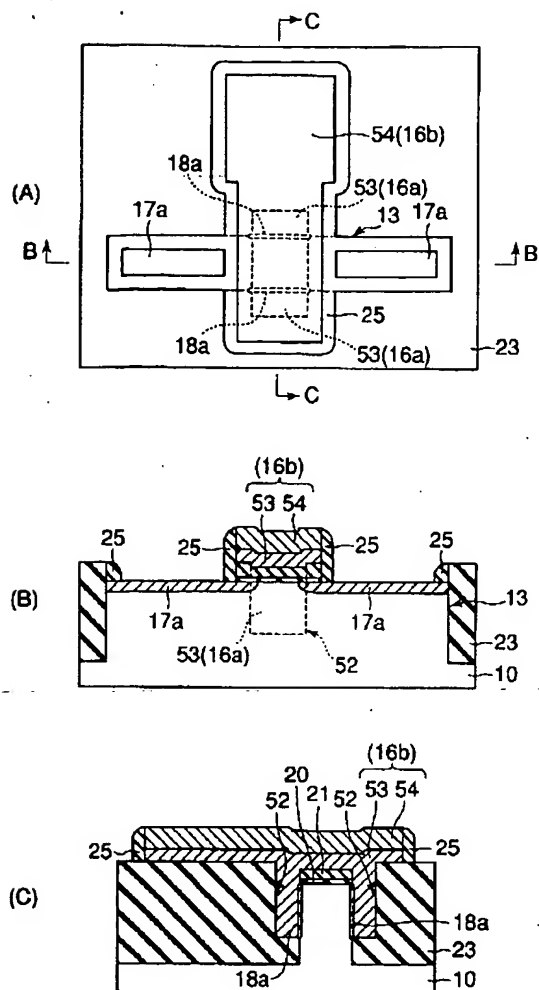
[Drawing 75]



[Drawing 76]

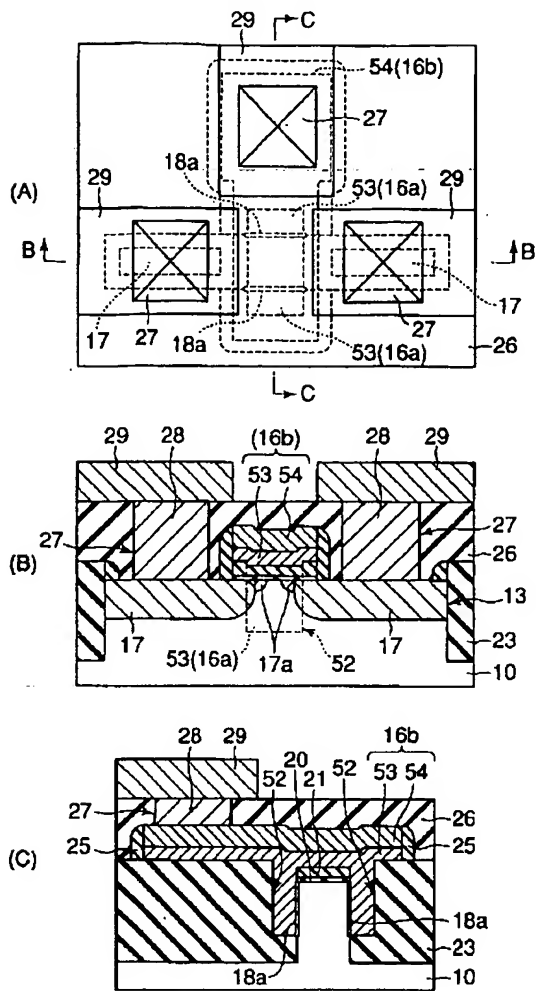


[Drawing 77]



[Drawing 78]





[Translation done.]

\* NOTICES \*

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention has the gate electrode which formed this invention in the side face of both sides through gate dielectric film about MOS transistor structure in the convex semi-conductor layer almost perpendicular to especially a substrate, and it is used for the MOS transistor structure where channel width is determined by the depth of the source / drain field, and its manufacture approach.

[0002]

[Description of the Prior Art] In the semiconductor device which has MOS mold structure, high performance-ization of MOSFET is a big technical problem. High performance-ization of MOSFET shows the increment in (1) drive current, reduction of (2) threshold variation, reduction of (3) parasitism resistance / parasitic capacitance, improvement in (4) cut-off characteristics, etc. In order to make a drive current increase, the gate dimension (it is also called a channel dimension and gate length) was shortened, and has been attained. However, when short channelization is carried out, there is also a problem said that the short channel effect increases.

[0003] In order to suppress the short channel effect, thickness of gate oxide was made as thin as possible, or high impurity concentration of the channel section was high-concentration-ized to about [  $10^{18}$  cm<sup>-3</sup> ] three, and efforts to prevent the punch-through between the source and a drain have been performed. However, thickness of gate oxide cannot be made thin beyond maximum-permissible electric field from the limit by the maximum-permissible electric field ( $E_{max}$ ) which can guarantee dependability.

[0004] Moreover, the problem that a drain current does not increase even if too much high concentration-ization of channel high impurity concentration brings about and carries out short channelization of the saturation of the drain current by dispersion of the high concentration impurity of a channel is becoming remarkable.

[0005] Furthermore, the increment in a raise in resistance of a gate electrode or parasitism resistance of the source/drain is posing a problem with detailed-izing. Moreover, further, since the punch-through between the source and a drain is easy to happen, leakage current increases in a subthreshold level field, and a cut-off characteristic is deteriorating.

[0006] In order to solve such a problem, a convex type rectangular parallelepiped is formed in Si substrate \*\*\*\* perpendicular, and the structure using the both-sides side is proposed as a channel field.

[0007] For example, IEDM Technical Digest A little side face which carried out STI (Shallow Trench Isolation) separation is exposed, and there is structure which uses a side face as a channel field as indicated by pp.736-739 (1987) (others [ Hieda / K ] ) ( drawing 79 ).

[0008] If channel width becomes small ( $<0.3$ micrometer), the depletion layer of the channel field of both sides will contact mutually under the effect of the gate electrode of a side face, the effect of the lateral portion which includes a corner rather than the flat-surface section becomes large, and the description of a cut-off characteristic improving is shown in this reference. However, the explanation about control of the short channel effect etc. is not shown.

[0009] Moreover, IEDM Technical Digest RIE of the Si substrate is carried out, a long and slender convex fence is formed, the lower part is oxidized, SOI structure is made, and the structure which forms the gate electrode of a both-sides side is proposed as indicated by pp.833-836 (1989) (D. others [ Hisamoto ] ) ( drawing 80 ).

[0010] If channel width becomes small ( $<0.2$ micrometer) also in this case, the depletion layer of the channel field of both sides will contact mutually under the effect of the gate electrode of a side face, and the condition of having depletion-ized completely is made in a channel field. That is, the same situation as the formation of perfect depletion in thin film SOI structure can be realized with Si substrate. However, this structure is SOI structure, it is the structure where substrate bias cannot be impressed and the physical relationship of the source/drain, and a gate electrode is not described.

[0011] Moreover, IEDM Technical Digest The structure of the fin mold using a SOI substrate is proposed as indicated by pp.1032-1034 (1998) (D. others [ Hisamoto ]) ( drawing 81 ).

[0012] It is shown by this reference by forming about 20nm Si fin (Fin) that the short channel effect is suppressed even to about 30nm channel length. However, it is the structure where substrate bias cannot be impressed like drawing 80 , because of SOI structure. Moreover, the thickness variation of a SOI layer is the structure of affecting MOSFET property variation directly.

[0013] In the device indicated by these reference, although the improvement of a cut-off characteristic and control of the short channel effect are realizable, since the seal of approval of the substrate bias cannot be carried out, degradation of the source / drain pressure-proofing under the effect of an are recording hole (in the case of an N channel) poses a problem like the case of the transistor of the thin film SOI with the channel formed into perfect depletion.

[0014] [Problem(s) to be Solved by the Invention] This invention was made in view of the above-mentioned actual condition, and that purpose is in the semiconductor device with the structure which can attain high performance-ization using a part of side face of a convex semi-conductor layer, and offering that manufacture approach as a channel field at least.

[0015] [Means for Solving the Problem] The convex semi-conductor layer prepared on the substrate in the 1st mode of the semiconductor device concerning this invention, The source field and drain field which were prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It provides and the distance between said source fields and said drain fields is changing in two side faces in which it faces mutually [ said convex semi-conductor layer ].

[0016] The convex semi-conductor layer prepared on the substrate in the 2nd mode of the semiconductor device concerning this invention, The source field and drain field which were prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and the side-attachment-wall insulator layer prepared on the side face of said gate electrode and the side face of said convex semi-conductor layer are provided.

[0017] The convex semi-conductor layer prepared on the substrate in the 3rd mode of the semiconductor device concerning this invention, The isolation insulator layer formed in the perimeter of the lower field of said convex semi-conductor layer, The source field and drain field which were prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to said channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It provides and the location of the top face of said isolation insulator layer is lower than the top face of said convex semi-conductor layer, and the location of the deepest part of said source field and a drain field is the same as the location of the top face of said component demarcation membrane, or lower than it.

[0018] The 1st convex semi-conductor layer which was prepared on the substrate and was electrically connected with this substrate in the 4th mode of the semiconductor device concerning this invention, Said 1st convex semi-conductor layer which was prepared on said substrate and was electrically connected with this substrate, and the 2nd convex semi-conductor layer with the same width of face, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, On the 1st side face of said 1st convex semi-conductor layer, and each 2nd side face of said 2nd convex semi-conductor layer in which this 1st side face was faced It has the side-attachment-wall gate section prepared in the condition of having insulated with these 1st and 2nd convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source fields and said 1st drain fields and the 2nd channel field between said 2nd source fields and said 2nd drain fields through said 1st side face and said 2nd side face is provided.

[0019] The 1st convex semi-conductor layer which was prepared on the substrate and was electrically connected with this substrate in the 5th mode of the semiconductor device concerning this invention, The 2nd convex semi-conductor layer which was prepared on said substrate and was electrically connected with this substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, It has the 1st side-attachment-wall gate section

prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, The 3rd wiring which connects the 2nd wiring which connects mutually the 1st wiring which connects mutually said 1st source field and said 2nd source field, and said 1st drain field and said 2nd drain field, and said 1st gate electrode and said 2nd gate electrode of each other is provided.

[0020] The 1st convex semi-conductor layer prepared on the substrate in the 6th mode of the semiconductor device concerning this invention, The 2nd convex semi-conductor layer prepared on said substrate, and the source field and drain field prepared in said 1st convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer, And it has the gate contact section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the top face of said 2nd convex semi-conductor layer, respectively. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer is provided.

[0021] The convex semi-conductor layer prepared on the substrate in the 7th mode of the semiconductor device concerning this invention, The source field and drain field which were prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. Providing the gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, the electric conduction object which constitutes said side-attachment-wall gate section differs from the electric conduction object which constitutes said top-face gate section.

[0022] The convex semi-conductor layer prepared on the substrate in the 8th mode of the semiconductor device concerning this invention, The source field and drain field which were prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, and wiring electrically contacted by said gate electrode in the top-face upper part of said convex semi-conductor layer are provided.

[0023] The 1st convex semi-conductor layer prepared on the substrate in the 9th mode of the semiconductor device concerning this invention, The 2nd convex semi-conductor layer prepared on said substrate, and the 1st source field and the 1st drain field prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which were prepared in said 2nd convex semi-conductor layer, On the 1st side face of said 1st convex semi-conductor layer, and each 2nd side face of said 2nd convex semi-conductor layer in which this 1st side face was faced It has the side-attachment-wall gate section prepared in the condition of having insulated with these 1st and 2nd convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source fields and said 1st drain fields, and the 2nd channel field between said 2nd source fields and said 2nd drain fields through said 1st side face and said 2nd side face, At least one 3rd convex semi-conductor layer of said 1st and 2nd source fields and said 1st and 2nd drain fields which connects either mutually at least is provided.

[0024] In the 10th mode of the semiconductor device concerning this invention The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field of the 1st conductivity type which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field of the 2nd conductivity type which were prepared in said 2nd convex semi-conductor layer, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field

between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, It provides and the depth of said 2nd source field and the 2nd drain field is deeper than the depth of said 1st source field and the 1st drain field.

[0025] In the 11th mode of the semiconductor device concerning this invention The 1st convex semi-conductor layer prepared on the substrate, and the 2nd convex semi-conductor layer prepared on said substrate, The 1st source field and the 1st drain field which were prepared in said 1st convex semi-conductor layer, The 2nd source field and the 2nd drain field which estrange mutually, are prepared in said 2nd convex semi-conductor layer, and have the same conductivity type as said 1st source field and said 1st drain field, It has the 1st side-attachment-wall gate section prepared in the condition of having insulated with this 1st convex semi-conductor layer, on the side face of said 1st convex semi-conductor layer. The 1st gate electrode which gives the electric field effect at least to the 1st channel field between said 1st source field and said 1st drain field through the side face of said 1st convex semi-conductor layer, It has the 2nd side-attachment-wall gate section prepared in the condition of having insulated with this 2nd convex semi-conductor layer, on the side face of said 2nd convex semi-conductor layer. The 2nd gate electrode which gives the electric field effect at least to the 2nd channel field between said 2nd source field and said 2nd drain field through the side face of said 2nd convex semi-conductor layer, It provides and the depth of said 2nd source field and the 2nd drain field is deeper than the depth of said 1st source field and the 1st drain field.

[0026] In the 12th mode of the semiconductor device concerning this invention The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It provides, said gate electrode is constituted including the 1st layer and the 2nd layer at least, and said gate electrode constitutes the word line of semiconductor memory equipment.

[0027] In the 13th mode of the semiconductor device concerning this invention The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It provides and said gate electrode is constituted including the 1st layer and the 2nd layer at least, said top face of the 1st layer is flat, and said 2nd layer is prepared on said flat top face of the 1st layer.

[0028] In the 14th mode of the semiconductor device concerning this invention The convex semi-conductor layer prepared on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, It has the side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer. The gate electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer, It provides and said gate electrode is constituted including the 1st layer and the 2nd layer at least, said top face of the 1st layer has a step, said 2nd layer is prepared on a top face with said step of the 1st layer, and said top face of the 2nd layer is flat.

[0029] In the 15th mode of the semiconductor device concerning this invention The convex semi-conductor layer which is prepared on a substrate and has the 1st side face, the 2nd side face which countered this 1st side face, the 3rd side face in which it is located between the 1st and 2nd side face, the 4th side face which countered this 3rd side face, and a top face, The source field and drain field which are prepared in said convex semi-conductor layer, and contain the electric contact section, respectively, It has the side-attachment-wall gate section prepared on the 1st side face at least in the condition of said convex semi-conductor layer of having insulated with this convex semi-conductor layer. The gate electrode which gives the electric field effect to the channel field between the gate electrode aforementioned source field which gives the electric field effect at least to the channel field between said source fields and said drain fields through the 1st side face of said convex semi-conductor layer, and said drain field is provided. said electric contact section -- a part of a part of 1st side face of each and said convex semi-conductor layer, a part of 2nd side face and top face, and 3rd and 4th side face -- either is straddled.

[0030] In the 16th mode of the semiconductor device concerning this invention The convex semi-conductor layer formed on the substrate, and the source field and drain field prepared in said convex semi-conductor layer, The side-attachment-wall gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the side face of said convex semi-conductor layer, And it has the top-face gate section prepared in the condition of having insulated with this convex semi-conductor layer, on the top face of said convex semi-conductor layer. The gate

electrode which gives the electric field effect at least to the channel field between said source fields and said drain fields through the side face of said convex semi-conductor layer is provided, and the gate length of said side-attachment-wall gate section is shorter than the gate length of said top-face gate section.

[0031] In the 1st mode of the manufacture approach of the semiconductor device concerning this invention The process which etches a semi-conductor substrate and forms a convex semi-conductor layer in this semi-conductor substrate, The process which forms gate dielectric film on the side face of said convex semi-conductor layer at least, The process which forms the gate electrode which has the part which met the side face of said convex semi-conductor layer at least on said gate dielectric film, The process which forms a side-attachment-wall insulator layer on the side face of said gate electrode, and the side face of said convex semi-conductor layer, Said gate electrode and said side-attachment-wall insulator layer are used for a mask at least, an impurity is introduced in said convex semi-conductor layer, and the process which forms a source field and a drain field in said convex semi-conductor layer is provided.

[0032] In the 2nd mode of the manufacture approach of the semiconductor device concerning this invention The process which forms the insulator layer which has puncturing on a semi-conductor substrate, and the process which forms a convex semi-conductor layer on the semi-conductor substrate exposed from said puncturing, The process which forms gate dielectric film on the side face of said convex semi-conductor layer at least, The process which forms the gate electrode which has the part which met the side face of said convex semi-conductor layer at least on said gate dielectric film, Said gate electrode is used for a mask at least, an impurity is introduced in said convex semi-conductor layer, and the process which forms a source field and a drain field in said convex semi-conductor layer is provided.

[0033] In the 3rd mode of the manufacture approach of the semiconductor device concerning this invention The process which forms a convex semi-conductor layer on a substrate, and the process which embeds the perimeter of said convex semi-conductor layer with an insulating material, The process which forms the slot for forming the side-attachment-wall gate section in said insulating material, The process which forms gate dielectric film on the side face of said convex semi-conductor layer exposed from said slot at least, The process which forms the gate electrode which has the side-attachment-wall gate section formed in said Mizouchi, and the process which uses said gate electrode for a mask at least, introduces an impurity in said convex semi-conductor layer, and forms a source field and a drain field in said convex semi-conductor layer are provided.

[0034]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained with reference to a drawing. On the occasion of this explanation, a common reference mark is given to the part which crosses and is common in a complete diagram.

[0035] (The 1st operation gestalt) The perspective view showing MOSFET which drawing 1 requires for the 1st operation gestalt of this invention, the sectional view where that top view and drawing 2 B meet the 2B-2B line in drawing 2 A in drawing 2 A, the sectional view where drawing 2 C meets the 2C-2C line in drawing 2 A, and drawing 2 D are sectional views which meet the 2D-2D line in drawing 2 A. In addition, in drawing 1 and drawing 2 B - drawing 2 D, the interlayer insulation film, contact, and wiring which are shown in drawing 2 A are omitted, respectively.

[0036] As shown in drawing 1 and drawing 2 A - drawing 2 D, the P type well 11 is formed in the transistor formation field of the P type Si (silicon) substrate 10. The P type Si substrate 10 has about [ 5x10<sup>15</sup>cm<sup>-3</sup> ] three high impurity concentration, and field bearing of the principal plane is (100). The P type high concentration impurity layer (following punch-through stopper layer) 12 with about [ 5x10<sup>17</sup>cm<sup>-3</sup> ] three high impurity concentration is formed in the transistor channel formation field in the P type well 11. It is also possible for this punch-through stopper layer 12 to be formed if needed, and to omit.

[0037] On the Si substrate 10, the convex thin film Si (silicon) layer 13 is formed (it is hereafter called a fence 13). The example of 1 design of a fence 13 is about 440nm in height of about 250nm, 70nm of \*\*\*\*, and die length. In the lower field of the fence 13 of this example, the upper part and the punch-through stopper layer 12 of the P type well 11 are contained, respectively. And the isolation insulator layer 14 for isolation (silicon oxide) is formed around this lower field.

[0038] On the punch-through stopper layer 12 in a fence 13, the channel impurity layer (channel field) 15 is formed. The impurity is doped by the channel impurity layer 15 so that the threshold electrical potential difference of MOSFET may become a desired value.

[0039] On both sides of the gate electrode 16, the source / drain field 17 is formed in the direction of a long side of a fence 13 (the die-length direction). The gate electrode 16 is formed so that the level difference of a fence 13 may be overcome through gate dielectric film 18 to the both-sides side of a fence 13. Channel width (Wg) is decided by width of face of the direction of a shorter side of a fence 13. Moreover, gate length (Lg) is mainly decided by the die length of



the gate electrode 16. However, effective channel length is decided by distance of the source / drain field 17 in the side face of the fence 13 of the gate electrode 16.

[0040] Furthermore, the gate electrode 16 is formed in the both-sides side and top face of a fence 13 the isolation insulator layer 14 top, and on these side faces and a top face, it is formed so that a part of a part of source / drain field 17, channel field 15, and punch-through stopper layer 12 may be covered.

[0041] Next, an example of the manufacture approach of MOSFET concerning the 1st operation gestalt is explained using the process sectional view of drawing 11 from drawing 3. In addition, the cross section shown in drawing 3 A - drawing 11 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 3 B - drawing 11 B is equivalent to the cross section shown in drawing 2 C.

[0042] First, as shown in drawing 3 A and drawing 3 B, the P type Si substrate 10 is prepared. this P type Si substrate 10 -- for example, about [  $5 \times 10^{15} \text{cm}^{-3}$  ] three high impurity concentration -- having -- field bearing of that principal plane -- for example, (100) -- it is .

[0043] When forming the N channel mold MOSFET (henceforth, NMOS) in the P type Si substrate 10, the ion implantation of the boron ion (B+) is carried out to the transistor channel formation field of the P type Si substrate 10 according to acceleration voltage 260KeV and 2 about [  $2 \times 10^{13} \text{cm}^{-2}$  dose to ] conditions. Thereby, the P type well 11 with about [  $4 \times 10^{17} \text{cm}^{-3}$  ] three peak concentration is formed in the P type Si substrate 10.

[0044] Moreover, in forming the P channel mold MOSFET (henceforth, PMOS) in the P type Si substrate 10, it forms an N type well (not shown) in the transistor channel formation field of the P type Si substrate 10.

[0045] Next, the resist film (not shown) is used for a mask, for example, the ion implantation of the boron ion (B+) is carried out into the P type well 11. Thereby, the high concentration impurity layer 12 with about [  $2 \times 10^{18} \text{cm}^{-3}$  ] three peak concentration is formed in the P type well 11. The high concentration impurity layer 12 functions as a punch-through stopper layer.

[0046] In addition, it is desirable at the time of a these ion grouting degree to form the oxide film (not shown) which has about 8nm thickness in the front face of the P type Si substrate 10. By forming the oxide film, the contamination, for example, metal contamination, to the P type Si substrate 10 from the above-mentioned resist film (not shown) can be prevented.

[0047] Moreover, RTA for about 5 minutes (Rapid Thermal Anneal) is used for activation of the poured-in ion in 900 degrees C and a nitrogen (N<sub>2</sub>) ambient atmosphere. The P type high concentration impurity layer 12 which has a steep profile by this can be formed.

[0048] Next, another resist film (not shown) is used for a mask, and the impurity ion of a desired conductivity type is poured into a field including the transistor channel formation field of the P type Si substrate 10. Thereby, the channel impurity layer 15 is formed in a transistor channel formation field. At this time, the channel impurity layer 15 may form impurity ion only in a transistor channel formation field by carrying out an ion implantation alternatively. When MOSFET formed wants to set the threshold electrical potential difference (V<sub>th</sub>) of this NMOS as about 0.7V by NMOS, the ion implantation of the boron ion (B+) is carried out to a transistor channel formation field according to acceleration voltage 20KeV and about [  $5 \times 10^{12} \text{cm}^{-2}$  ] two conditions. This ion implantation is performed through an oxide film (not shown). Thereby, the P type channel impurity layer 15 is formed in a transistor channel formation field. Moreover, in the field used as a channel, the P type channel impurity layer 15 is formed so that it may become a uniform profile alternatively. RTA may be used for activation of this P type channel impurity layer 15. An example of the conditions of RTA is about 10 seconds at the temperature of 750 degrees C.

[0049] Next, after removing the above-mentioned oxide film (not shown), sequential formation of the mask layer (SiN) 21 which has again the thickness of 20 or about 20nm of SiO<sub>2</sub> two-layer which has about 5nm thickness on the front face of the P type Si substrate 10, and the mask layer (SiO<sub>2</sub>) 22 with about 20nm thickness is carried out. then, lithography and RIE -- using -- SiO<sub>2</sub> two-layer -- 20, the mask layer 21, and the mask layer 22 are processed into a desired configuration, for example, the configuration used as the active area of MOSFET.

[0050] Next, using as the mask of etching [ the Si substrate 10 ] of the mask layer 22 structure shown in drawing 3 A and drawing 3 B using RIE, as shown in drawing 4 A and drawing 4 B, it etches until it reaches in the middle of the P type well 11. Thereby, a slot with a depth of about 250nm and a fence 13 are formed in the Si substrate 10 at coincidence. A fence 13 is a field in which the source of MOSFET, a drain, and a channel are formed, respectively. an example of the height of a fence 13 -- for example, the depth of flute -- the same -- it is about 250nm.

[0051] Next, while cleaning the side face of a fence 13, and the bottom of a slot using ashing, wet processing, etc., the part which received the damage by RIE among the Si substrates 10 is removed. Thereby, Si front face with few damages is exposed to the side face of a fence 13, or the bottom of a slot. Next, the oxide film (not shown) which has about 7nm thickness in the side face of a fence 13 or the bottom of a slot is formed. One to form this oxide film is

making an interface property good. Furthermore, as for this oxide film, it is desirable to form with the radical oxidation style which used the oxygen radical. A radical oxidation style is because a good oxide film can be formed at about low temperature, for example, 700 degrees C.

[0052] Next, as shown in drawing 5 A and drawing 5 B, Mizouchi in whom the above-mentioned oxide film (not shown) was-formed is filled up with an insulating material 23. Thereby, a slot is embedded with an insulating material 23 and the so-called shallow trench isolation (Shallow Trench Isolation) is formed in the Si substrate 10. An example of an insulating material 23 is SiO<sub>2</sub>. Moreover, a desirable example of SiO<sub>2</sub> is TEOS-SiO<sub>2</sub> which used TEOS for reactant gas and formed it.

[0053] The following of an example of the concrete manufacture approach of STI is carried out.

[0054] First, about 500nm of TEOS-SiO<sub>2</sub> is deposited on the structure shown in drawing 4 A and drawing 4 B using the CVD method which made reactant gas to TEOS and made membrane formation temperature about 650 degrees C. thereby -- TEOS-SiO two-layer (insulating material) -- 23 is formed. next, TEOS-SiO two-layer -- 23 is densified by the radical oxidizing atmosphere with a temperature of about 700 degrees C. then, CMP (Chemical Mechanical Polishing) -- law -- using -- TEOS-SiO two-layer -- flattening of the front face of 23 is carried out. this time -- the CMP rate of the mask layer (SiN) 21, and TEOS-SiO two-layer -- a difference with the CMP rate of 23 -- TEOS-SiO two-layer -- 23 is embedded evenly at Mizouchi.

[0055] Moreover, TEOS-O<sub>3</sub>-SiO<sub>2</sub> formed using TEOS-O<sub>3</sub> CVD method besides above-mentioned TEOS-SiO<sub>2</sub> as a desirable example of an insulating material 23 and the HDP-SiO<sub>2</sub> grade formed using the HDP (HighDensity Plasma) CVD method can be mentioned.

[0056] next, it is shown in drawing 6 A and drawing 6 B -- as -- for example, the RIE method -- using -- TEOS-SiO two-layer -- etchback of 23 is carried out. Thereby, the isolation insulator layer 14 with about 100nm thickness for isolation is formed in the pars basilaris ossis occipitalis of a slot.

[0057] Next, as shown in drawing 7 A and drawing 7 B, the mask layer (SiN) 21 is removed using hot phosphoric acid etc. subsequently, the SiO two-layer currently formed on the oxide film (not shown) currently formed on the side face of a fence 13, and the side face of a fence 13 -- 20 is removed using the solution of a fluoric acid system. Thereby, Si is exposed from the side face of a fence 13, and its top face. Subsequently, gate dielectric film 18 is formed on the front face of exposed Si. The desirable example of formation of gate dielectric film 18 is that about 2.5nm oxidizes the front face of exposed Si using an about 700-degree C radical oxidation style.

[0058] It is hard to depend for a radical oxidation style on field bearing of a fence 13. For this reason, unevenness can realize little gate dielectric film 18. MOSFET in which unevenness has little gate dielectric film 18 has few falls of channel MOBIRITI for example, by channel interface dispersion, and is powerful.

[0059] Furthermore, at a certain temperature, there is the description that only SiO<sub>2</sub> film of a certain fixed thickness can be formed in a radical oxidation style. For this reason, there is an advantage that thickness variation in the wafer side of gate dielectric film 18 and variation during the chip of gate dielectric film 18 can be made small, respectively.

[0060] Of course, not only SiO<sub>2</sub> film formed using the radical oxidation style but the SiON film and the so-called oxy-night RAIDO film may be used for gate dielectric film 18. The oxy-night RAIDO film can form the usual thermal oxidation film for example, using the oxidizing [ thermally ] method, and can form it by nitriding the front face by the gas containing nitrogen further.

[0061] Furthermore, SiO<sub>2</sub> film and not only the SiON film but the so-called high dielectric insulator layer (high-kappa film) may be used for gate dielectric film 18. An example of MOSFET which used the high-kappa film is shown in gate dielectric film 18 at drawing 24 .

[0062] As an example of the high-kappa film, 2OTa5 film (the so-called tantalum oxide), 2Oaluminum3 film, 2OLa3 film, HfO<sub>2</sub> film, ZrO<sub>2</sub> film, etc. can be mentioned.

[0063] Specific-inductive-capacity epsilon of 2OTa5 film is [ about 20 to about 27 ] especially large compared with specific-inductive-capacity epsilon=3.9 of a \*\*\*\* and SiO<sub>2</sub> film. For this reason, 2OTa5 film is film as for which oxide-film conversion thickness (equivalent film thickness) when converting thickness into SiO<sub>2</sub> film may be made to 2nm or less.

[0064] Moreover, when using 2OTa5 film for gate dielectric film 18, after forming the film of about 1nm Si oxide-film system in Si interface, it is good also as the so-called laminating gate-dielectric-film structure which forms 2OTa5 film on it. According to such laminating gate-dielectric-film structure, the interface-state-density consistency of gate dielectric film and Si interface can be reduced.

[0065] Next, as shown in drawing 8 A and drawing 8 B, on the structure shown in drawing 7 A and drawing 7 B, the polycrystal Si with which for example, the N type impurity was doped is deposited on about 100nm, and the doped polycrystal Si film is formed. The doped polycrystal Si film serves as the gate electrode 16 behind. Subsequently, an



SiN film is deposited on the doped polycrystal Si film at about 100nm. This SiN film turns into the gate cap insulator layer 24 behind. Subsequently, the resist film (not shown) is used for a mask, first, the gate cap insulator layer (SiN) 24 is etched, subsequently to a mask the gate cap insulator layer (SiN) 24 is used, and the doped polycrystal Si film is etched. Thereby, the gate electrode 16 is formed. At this time, the gate electrode 16 is processed ranging over a fence 13. For this reason, it is important for the doped polycrystal Si film to etch the ratio (selection ratio) of the etching rate of this doped polycrystal Si film and an etching rate with gate dielectric film 18 using the conditions which can fully be taken, for example, conditions which have about 400. By using such conditions, it can prevent that the damage by etching joins a fence 13.

[0066] Moreover, it is possible to use the laminating gate structure of not only the doped polycrystal Si film but the metal film or the metal film, and the metal film, the laminating gate structure (the so-called poly metal structure) of the polycrystal Si film and the metal film, or the laminating gate structure (the so-called polycide structure) of the polycrystal Si film and the silicide film for the gate electrode 16. According to the gate electrode 16 using metal structure, the laminating gate structure of the metal film and the metal film, the poly metal structure, and polycide structure, resistance of the gate electrode 16 can be reduced compared with the gate electrode only using the doped polycrystal Si film.

[0067] As an example of the metal film, the TiN film, W film, WN film, Ru film, Ir film, aluminum film, etc. can be mentioned.

[0068] As an example of the silicide film, although CoSi<sub>2</sub> film, TiSi<sub>2</sub> film, etc. are mentioned, things are made.

[0069] Moreover, when the gate electrode 16 is constituted for example, using the TiN film, there is the description that the work function of the gate electrode 16 can be changed by adjusting the stacking tendency of the TiN film etc. For this reason, it also becomes possible to adjust the threshold electrical potential difference of MOSFET because the work function of the gate electrode 16 makes it change.

[0070] Moreover, the die length (the so-called gate length) of the gate electrode 16 is set to about 70nm. In this invention, although mentioned later in detail, since the short channel effect of PMOSFET can be controlled, you may design so that the both sides of NMOS and PMOS may use the same channel length.

[0071] Next, on the structure shown in drawing 8 A and drawing 8 B, a CVD method is used and an insulating material, for example, SiO<sub>2</sub> and SiN, is deposited. Subsequently, RIE of the deposited insulating material is carried out, and it leaves this insulating material on the side attachment wall of the gate electrode 16, and the side attachment wall of a fence 13. Thereby, the side-attachment-wall insulator layer 25 which has about 20nm thickness in the side attachment wall of the gate electrode 16 and each side attachment wall of a fence 13 is formed.

[0072] Next, the gate cap insulator layer 24, the gate electrode 16, and the side-attachment-wall insulator layer 25 are used for a mask, for example, the ion implantation of the arsenic ion (As<sup>+</sup>) is carried out into a fence 13 according to acceleration voltage 20KeV and 2 about [ 5x10<sup>15</sup>cm dose to ] conditions. Thereby, the N type source / drain field 17 is formed in a fence 13.

[0073] before [ moreover, ] forming the side-attachment-wall insulator layer 25 -- the gate electrode 16 -- for example, RTO of a radical oxidation style or low temperature -- the oxide film (not shown) which oxidizes using law etc., for example, has about 2nm thickness may be formed. One of the purposes of this oxide film is easing the electric-field concentration in the side attachment wall and pars-basilaris-ossis-occipitalis corner of the gate electrode 16.

[0074] Moreover, although this example described the single source / drain structure, it is also possible to use the so-called extension structure which constituted the source / drain field 17 from N-mold diffusion layer 17a and N<sup>+</sup> mold diffusion layer 17b. An example of MOSFET using extension structure is shown in drawing 29 .

[0075] As shown in drawing 29 , the gate cap insulator layer 24, the gate electrode 16, and the side-attachment-wall insulator layer 25 are used for a mask, for example, the ion implantation of the phosphorus ion (P<sup>+</sup>) is carried out into a fence 13 according to acceleration voltage 40KeV and 2 about [ 4x10<sup>13</sup>cm dose to ] conditions. This forms N-mold diffusion layer 17a in a fence 13. Of course, N-mold diffusion layer 17a may be formed by carrying out the ion implantation not only of phosphorus ion but the arsenic ion etc. into a fence 13.

[0076] By the way, control of the depth (X<sub>j</sub>) of the N type source / drain field 17 is an important process. It is because it is the process which determines the channel width of a convex Si transistor. Cautions are especially required for a temperature setup of heat treatment including activation of the impurity of the N type source / drain field 17 etc.

[0077] The depth (X<sub>j</sub>) of the N type source / drain field 17 is controlled by the thermal activation after the final ion-implantation stratification, and heat treatment conditions. For example, an ion notes entry condition (acceleration voltage and dose) and thermal activation conditions are controlled, and it realizes so that it may become about PN-junction depth (X<sub>j</sub>) = 0.12micrometer.

[0078] In this example, the offset field used as the gate electrode 16 and offset exists in a lower part among the N type

source / drain field 17 exposed on the side face of a fence 13. This originates in forming the N type source / drain field 17 by the ion implantation to the front face of a fence 13, especially a top face, and thermal diffusion. According to the N type source / the drain field 17 with such an offset field, generating of the punch-through in the field of the lower part of the N type source / drain field 17 can be controlled especially. Moreover, like this example, if the punch-through stopper layer 12 is further formed in the lower field of the N type source / drain field 17, generating of the punch-through in the lower field of the above-mentioned N type source / drain field 17 can be controlled still more effectively.

[0079] In addition, in this example, at the time of an ion implantation to form the N type source / drain field 17, since the side face of a fence 13 is covered with the side-attachment-wall insulator layer 25, the ion implantation to the top face of a fence 13 becomes main, and the ion implantation of the impurity to a side face has structure which can be prevented. However, the side-attachment-wall insulator layer 25 is not necessarily required.

[0080] Moreover, when it is necessary to reduce the specific resistance of the N type source / drain field 17, a silicide layer (not shown) may be formed in the front face of the N type source / drain field 17 to make specific resistance lower than 50micro ohm-cm extent.

[0081] as the example of a silicide layer --  $\text{TiSi}_2$ ,  $\text{CoSi}_2$ ,  $\text{PtSi}$ , and  $\text{Pd}_2\text{Si}$  --  $\text{Si}$ ,  $\text{IrSi}_3$ ,  $\text{RhSi}$ , etc. can be mentioned.  $\text{Pd}_2\text{Si}$  is effective in order to reduce contact resistance of this P type source / drain field 17 especially, when the source / drain field 17 is P type.

[0082] Next, as shown in drawing 10 A and drawing 10 B, on the structure shown in drawing 9 A and drawing 9 B, a CVD method is used and about 500nm of  $\text{SiO}_2$  is deposited, for example. Thereby, an interlayer insulation film 26 is formed. Then, it is an about 700-degree C radical oxidizing atmosphere, for example, an interlayer insulation film 26 is densified about 30 minutes. Like this heat process, you may carry out to serve also as activation of the ion-implantation layer of the N type source / drain field 17. Temperature of densifying is low-temperature-ized or RTA of msec order extent may be performed at about 850 degrees C to control the depth ( $X_j$ ) of the N type source / drain field 17. Furthermore these may be used together and the ion-implantation layer of the N type source / drain field 17 may be activated. Then, flattening of the interlayer insulation film 26 is carried out using the CMP method.

[0083] Next, as shown in drawing 11 A and drawing 11 B, a contact hole 27 is formed in an interlayer insulation film 26 using lithography and RIE. Next, it is filled up with W (tungsten) film, aluminum (aluminum) film,  $\text{TiN}$  (titanium nitride) film /  $\text{Ti}$  (titanium) film, or those cascade screens in a contact hole 27. Thereby, the contact plug 28 is formed in a contact hole 27. Next, the wiring layer 29 which contacts the contact plug 28 electrically is formed on an interlayer insulation film 26. A wiring layer 29 consists of electric conduction objects which used aluminum as the principal component. Next, the basic structure of MOSFET concerning the 1st operation gestalt of this invention completes the passivation film (not shown) by depositing an interlayer insulation film 26 and a wiring layer upwards.

[0084] The following of the typical effectiveness is carried out among the effectiveness acquired from MOSFET concerning such a 1st operation gestalt.

[0085] (1) Separate the source / drain field 17 formed into the fence 13 from the isolation insulator layer 14 formed in the lower field of this fence 13. Thereby, the channel width of MOSFET is controllable by the depth of the source / drain field 17. For this reason, the effect of the variation in the etching depth of a slot produced in case a fence 13 is formed can realize structure where the variation in channel width is not influenced.

[0086] (2) Make width of face ( $W_g$ ) of a fence 13 narrower than 0.20 micrometers. The channel impurity layer 15 can be completely depletion-ized with the gate electrode 16 which this formed on two side faces in which the fence 13 faced mutually. The short channel effect can be controlled by depletion-izing the channel field 15 completely.

[0087] (3) Form the high concentration impurity layer (punch-through stopper layer) 12 between the channel field 15 of a fence 13, and a well 11 (or  $\text{Si}$  substrate 10). Thereby, the punch-through between the source/drain can be prevented.

[0088] (4) Make distance between the source / drain field 17 exposed on the side face of a fence 13 into the configuration which spreads as it is narrow in the side-face upper part and becomes the side-face lower part. Thereby, the punch-through between the source/drain can be prevented.

[0089] (5) In addition to (4), make a part of source / drain field 17 exposed on the side face of a fence 13 into an extremely different configuration from the former which became outside in [ electrode / 16 / gate ] self align. This offsets the parts of a part of source / drain field 17, for example, the lower part of the source / drain field, from the gate electrode 16. Thus, by giving an offset field to the source / drain field 17, the punch-through between the source/drain, especially the punch-through in the field of the lower part between the source/drain can be prevented.

[0090] (6) Although a part of channel field 15 of MOSFET is the structure acquired on the side face of a fence 13, the contact to the source / drain field 17, the contact to the gate electrode 16, and wiring are formed in the flat surface 26 by which flattening was carried out nearly completely, for example, an interlayer insulation film, and on an interlayer

insulation film 26. For this reason, it is possible to use the process technique of the conventional planar mold MOSFET as it is.

[0091] (The 2nd operation gestalt) The perspective view showing MOSFET which drawing 12 requires for the 2nd operation gestalt of this invention, drawing 13 A, and drawing 13 B are that sectional view, respectively. In addition, the cross section shown in drawing 13 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 13 B is equivalent to the cross section shown in drawing 2 C. Moreover, in drawing 12 and drawing 13 A and drawing 13 B, the contact and wiring which were shown in drawing 2 A are omitted, respectively.

[0092] The 1st operation gestalt showed the structure which used gate dielectric film 18 with almost equal thickness in respect of the top face of a fence 13, and both sides.

[0093] The \*\*\*\* 2 operation gestalt shows structure with thick gate-dielectric-film (TOP insulator layer) 18b of thickness to the top face of a fence 13 compared with gate-dielectric-film 18a of a both-sides side, as shown in drawing 12 and drawing 13 A and drawing 13 B.

[0094] By using such structure, in the channel field 15 of a fence 13, the gate electric-field concentration in an up corner can be eased, and the effect can be reduced. Thus, by the ability of the effect of gate electric-field concentration to be reduced, fluctuation of the threshold electrical potential difference when impressing fluctuation of the threshold electrical potential difference resulting from gate electric-field concentration and fluctuation of a substrate bias property, i.e., substrate bias, can be controlled.

[0095] the SiO two-layer formed on the top face of a fence 13 in the process explained with reference to drawing 6 A of the 1st operation gestalt, and drawing 6 B in order to have acquired such structure -- it leaves without removing 20, and gate-dielectric-film 18a is formed on the side face of a fence 13 after that. Thereby, on the top face of a fence 13, the gate-dielectric-film structure which has two kinds of thickness thin gate-dielectric-film 18a, on thick gate-dielectric-film 18b and the both-sides side of a fence 13 is realizable.

[0096] In addition, as shown not only in SiO<sub>2</sub> film but in drawing 25, the thing of a \*\*\*\* 2 operation gestalt for which the so-called high dielectric insulator layers (high-kappa film), such as 2OTa5 film, HfO<sub>2</sub> film, and ZrO<sub>2</sub> film, are used is especially possible for gate-dielectric-film 18a.

[0097] Moreover, after forming the film of about 1nm Si oxide-film system in Si interface when 2OTa5 film is used for gate-dielectric-film 18a in order to reduce an interface-state-density consistency with Si interface for example, it is good also as the so-called cascade screen gate-dielectric-film structure which forms 2OTa5 film on it.

[0098] In addition, as for the deformation which uses the above-mentioned quantity dielectric insulator layer (high-kappa film) for gate-dielectric-film 18a, it is needless to say for it to be able to apply with all the operation gestalten explained on these specifications.

[0099] (The 3rd operation gestalt) Drawing 14 A and drawing 14 B are the sectional views showing MOSFET concerning the 3rd operation gestalt of this invention, respectively. In addition, the cross section shown in drawing 14 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 14 B is equivalent to the cross section shown in drawing 2 C. Moreover, in drawing 14 A and drawing 14 B, the contact and wiring which were shown in drawing 2 A are omitted, respectively.

[0100] The 1st operation gestalt showed the example of structure to which the punch-through stopper layer 12 exists between the sources / drain fields 17, and the wells 11 (or Si substrate 10) which were formed into the fence 13.

[0101] As a \*\*\*\* 3 operation gestalt shows to drawing 14 A and drawing 14 B, the depth of the source / drain field 17 is deeper than the 1st operation gestalt. For example, by this example, the pars basilaris ossis occipitalis of the source / drain field 17 is almost equal to the top face of the isolation insulator layer 14 formed in the perimeter of a fence 13, or the case of being deeper than it is shown. In this case, since the gate electrode 16 is formed along the side face of a fence 13 from the top face of the isolation insulator layer 14, the location of the pars basilaris ossis occipitalis of the source / drain field 17 and its location of the gate electrode 16 will correspond mostly.

[0102] With such structure, since the depth of the source / drain field 17 can be made deep, channel width can be enlarged. Therefore, the height of a fence 13 can be made low and the effectiveness that processing of the gate electrode 16 is easy can be acquired.

[0103] (The 4th operation gestalt) Drawing 15 A and drawing 15 B are the sectional views showing MOSFET concerning the 4th operation gestalt of this invention, respectively. In addition, the cross section shown in drawing 15 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 15 B is equivalent to the cross section shown in drawing 2 C. Moreover, in drawing 15 A and drawing 15 B, the contact and wiring which were shown in drawing 2 A are omitted, respectively.

[0104] The 1st operation gestalt showed the example of structure which the punch-through stopper layer 12 existed between the sources / drain fields 17, and the wells 11 (or Si substrate 10) which were formed into the fence 13, and the

source / drain field 17 has offset with the gate electrode 16 in the side face of a fence 13.

[0105] With the \*\*\*\* 4 operation gestalt, as shown in drawing 15 A and drawing 15 B, the depth of the source / drain field 17 is deeper than the 1st operation gestalt, and shows structure without an offset field. By this example, the pars basilaris ossis occipitalis of the source / drain field 17 is almost equal to the top face of the isolation insulator layer 14 formed in the perimeter of a fence 13, is deeper than it, and, specifically, overlaps the source / drain field 17 completely with the gate electrode 16 in the side face of a fence 13. What is necessary is to use the gate electrode 16 and its side-attachment-wall insulator layer 25 for a mask, and just to form the source / drain field 17 by solid phase diffusion from the film which doped the impurity, in order to acquire such structure.

[0106] With such structure, since the source / drain field 17 can be formed to a deep field and big channel width can be realized like the 3rd operation gestalt, the height of a fence 13 can be made low and the effectiveness that processing of the gate electrode 16 becomes easy can be acquired.

[0107] (The 5th operation gestalt) The top view showing MOSFET which drawing 16 A requires for the 5th operation gestalt of this invention, the sectional view where drawing 16 B meets the 16B-16B line in drawing 16 A, and drawing 16 C are sectional views which meet the 16C-16C line in drawing 16 A.

[0108] The 1st operation gestalt described the case where the number of fences 13 was one.

[0109] With a \*\*\*\* 5 operation gestalt, in order to realize bigger channel width, two or more fences 13 are doubled and the case where one MOSFET is formed is stated.

[0110] As shown in drawing 16 A - drawing 16 C, a fence 13 is arranged to juxtaposition, and contact of the source / drain field 17 HE is carried out in common, and the gate electrode 16 is also carried out in common. Thereby, big channel width is realizable.

[0111] Since the side face of a fence 13 can be used as channel width, compared with MOSFET with superficial structure, superficial area can be made small.

[0112] Moreover, the contact to the gate electrode 16 can be formed in the part arranged on the isolation insulator layer 14 among the gate electrodes 16 at this time.

[0113] Bigger channel width is realizable in a fewer superficial area arranging two or more fences 13, carrying out the source, a drain, and the gate in common with the structure concerning a \*\*\*\* 5 operation gestalt, and making it operate as one transistor. There are the features that the densification of a semiconductor integrated circuit is realizable by this. As for the width of face of two or more thin film convex Si layers 13, at this time, it is desirable to suppose respectively that it is almost the same, and to be arranged mutually. It is because each MOSFET property can be made the same if it is the same width of face.

[0114] Moreover, you may make it arrange respectively the width of face of the thin film convex Si layer 13 similarly in two or more MOSFETs of all formed into one chip, or its part from a viewpoint that width of face of two or more thin film convex Si layers 13 is respectively made almost the same, and each MOSFET property can be made the same by arranging mutually.

[0115] Thus, if the width of face of two or more thin film convex Si layers 13 is arranged, the advantage of becoming easy to form two or more thin film convex Si layers 13 minutely, for example can be acquired.

[0116] It is because it will be easy to process the thin film convex Si layer 13 and embedding will also become easy, if the width of face of the thin film convex Si layer 13 has gathered. Consequently, the manufacture yield of a component improves. This advantage will be very useful from now on for detailed-izing of MOSFET progress is further expected to be, and high integration of semiconductor integrated circuit equipment.

[0117] Moreover, in two or more MOSFETs accumulated by semiconductor integrated circuit equipment, a difference is in the drive capacity needed, respectively on circuitry.

[0118] Conventionally, it succeeded in accommodation of drive capacity by changing channel width. Changing channel width means modification of the width of face of the component field in which MOSFET is formed. For this reason, in the conventional semiconductor integrated circuit, the component field of various width of face was accumulated into 1 chip. Such structure is not a not much desirable thing for detailed-izing of MOSFET with which are hard to form minutely and progress is further expected to be, and high integration of semiconductor integrated circuit equipment.

[0119] However, with the semiconductor integrated circuit equipment formed using MOSFET concerning this invention, it becomes possible to arrange possible [ arranging the width of face of the thin film convex Si layer 13 with the conventional component field considerable the bottom ], and ultimately [ all ]. It is possible to arrange the width of face of all the thin film convex Si layers 13 ultimately.

[0120] In MOSFET concerning this invention, it is because channel width can be changed like a \*\*\*\* 5 operation gestalt by carrying out the gate electrode 16 in common in two or more thin film convex Si layers 13 and accommodation of drive capacity is attained by this.

[0121] (The 6th operation gestalt) The top view showing MOSFET which drawing 17 A requires for the 6th operation gestalt of this invention, the sectional view where drawing 17 B meets the 17B-17B line in drawing 17 A, and drawing 17 C are sectional views which meet the 17C-17C line in drawing 17 A.

[0122] With the 5th operation gestalt, in order to realize bigger channel width, two or more fences 13 were doubled and the case where one MOSFET was formed was stated. Moreover, the contact to the gate electrode 16 described the case where it formed in the part arranged on the isolation insulator layer 14 among the gate electrodes 16.

[0123] The place where a \*\*\*\* 6 operation gestalt differs from the 5th operation gestalt is the structure of taking the contact to the gate electrode 16.

[0124] As shown in drawing 17 A - drawing 17 C, the convex thin film Si layer 30 for taking contact is formed independently [ a fence 13 ], and the gate electrode 16 is extended to the top face of the convex thin film Si layer 30. And contact is taken to the gate electrode 16 in the upper part of the top face of the convex thin film Si layer 30.

[0125] The magnitude of the convex thin film Si layer 30 for this gate contact is easy to be the magnitude which can take contact. And the purpose of the convex thin film Si layer 30 is to reduce the difference of the contact depth to the source / drain field 17 of MOSFET, and the contact depth to the gate electrode 16 of MOSFET. By considering as structure with such a convex thin film Si layer 30, it becomes possible to obtain the stable contact and it can improve the manufacture yield.

[0126] According to the structure concerning a \*\*\*\* 6 operation gestalt, the contact to the gate electrode 16 can be taken in the upper part of the top face by forming the convex thin film Si layer 30 for gate contact formation. Deep contact can be avoided by this and it comes to be able to perform contact and manufacture by which the wiring process was stabilized.

[0127] Drawing 18 A and drawing 18 B are the sectional views showing MOSFET concerning the other examples of the 6th operation gestalt of this invention, respectively. In addition, the cross section shown in drawing 18 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 18 B is equivalent to the cross section shown in drawing 2 C.

[0128] As shown in drawing 18 A and drawing 18 B, the structure concerning the 6th operation gestalt can be applied also in structure with one MOSFET like the 5th operation gestalt not only like structure with two or more MOSFETs but like the 1st operation gestalt.

[0129] Also in this case, formation of deep contact can be avoided to the gate electrode 16 by taking contact, and manufacture by which contact and a wiring process were stabilized comes be made to it in the upper part of the top face of the convex thin film Si layer 30 for gate contact formation.

[0130] (The 7th operation gestalt) Drawing 19 A and drawing 19 B are the sectional views showing MOSFET concerning the 7th operation gestalt of this invention, respectively.

[0131] The 1st operation gestalt described the example which formed the fence 13 so that it might have an almost perpendicular include angle to the Si substrate 10.

[0132] With a \*\*\*\* 7 operation gestalt, as shown in drawing 19 A and drawing 19 B, in order to make easy processing of the formal gate electrode over the fence 13 used as a level difference, it forms so that it may have the forward tapered shape include angle theta in a fence 13. for example, compared with the case of being perpendicular, it also boils markedly having given the forward tapered shape include angle theta of about 1 - 3 times to the fence 13, and, as for processing of the gate electrode 16, it can carry out [ easy ]-izing.

[0133] Moreover, what is necessary is just to adjust etching conditions, in case the mask layer 22 explained with reference to drawing 4 [ of the 1st operation gestalt ] A and drawing 4 B is used for the mask of etching and the Si substrate 10 is etched, in order to form a fence so that it may have this cone-angle theta for example. It is comparatively easy to give the forward tapered shape include angle of 1 - 3 times.

[0134] Thus, the effectiveness that-izing of the processing of the gate electrode 16 can be carried out [ easy ], and the dimension conversion difference at the time of this processing can be made small can be acquired by making a fence 13 into forward tapered shape structure.

[0135] (The 8th operation gestalt) The perspective view showing MOSFET which drawing 20 requires for the 8th operation gestalt of this invention, the sectional view where that top view and drawing 21 B meet the 21B-21B line in drawing 21 A in drawing 21 A, and drawing 21 C are sectional views which meet the 21C-21C line in drawing 21 A.

[0136] With the 1st operation gestalt, the gate electrode 16 which consists of one pattern showed the example currently formed along the both-sides side ranging over the top face of a fence 13.

[0137] Similarly, with the 5th operation gestalt, the gate electrode 16 which consists of one pattern showed the example currently formed along those both-sides sides respectively ranging over the top face of two or more fences 13.

[0138] A \*\*\*\* 8 operation gestalt constitutes the gate electrode 16 with two or more patterns of 2nd gate electrode 16b



which touches 1st gate electrode 16a which touches gate-dielectric-film 18a formed in the side face of a fence 13, and gate-dielectric-film (TOP insulator layer) 18b formed in the top face of the film Si layer 13, as shown in drawing 20 and drawing 21 A - drawing 21 C. In addition, in this example, gate-dielectric-film (TOP insulator layer) 18b is taken as a thing thicker than gate-dielectric-film 18a like the 2nd operation gestalt.

[0139] 1st gate electrode 16a is formed in the 1st side face of a fence 13; and the 2nd side face which faced this 1st side face according to the individual, respectively. And each [ these ] 1st gate electrode 16a is connected in the metal layer for connection used as 2nd gate electrode 16b. Here, 2nd gate electrode 16b of making it function as a gate electrode of MOSFET is also possible, and it is possible to make thick enough 2nd gate-dielectric-film (TOP insulator layer) 18b, and to also make it function as wiring simply. When it is made to function as wiring simply, the gate electrode of the 1st MOSFET formed in the 1st side face and the gate electrode of the 2nd MOSFET formed in the 2nd side face which faced the 1st side face are mutually connected with wiring, and it can be said as the structure it was made to operate these two MOSFETs as one MOSFET.

[0140] In order to form the structure concerning a \*\*\*\* 8 operation gestalt, it is realizable by using for the mask of etching of gate-dielectric-film (TOP insulator layer) 18b, leaving the electric conduction object set to 1st gate electrode 16a at the side attachment wall of fence 13a by the side-attachment-wall remnants method using the RIE method, using the resist film for a mask after that, and processing the configuration of gate electrode 16a. At this time, gate-dielectric-film (TOP insulator layer) 18b formed in the top face of a fence 13 can use it as a mask of etching at the time of RIE, and also the etching damage at the time of RIE prevents going into a fence 13. Thus, in the structure concerning the operation gestalt of \*\*\*\* 8, gate-dielectric-film (TOP insulator layer) 18b plays an important role especially.

[0141] Moreover, although possibility that doubling gap will occur is between 1st gate electrode 16a and 2nd gate electrode 16b, it is uninfluent to the electrical property of MOSFET.

[0142] By taking the electrode structure concerning such 8th operation gestalt, the Pori Si layer which doped the ingredient of 1st gate electrode 16a, for example, an impurity, only on the side attachment wall of a fence 13 can be formed. For this reason, there are the features that the ingredient of a gate electrode can be changed according to the electrical property of MOSFET.

[0143] Moreover, if the metal layer used as 2nd gate electrode 16b is formed by the cascade screen of W film / TiN film / Ti film of about 100nm of thickness etc. even if it thin-film-izes thickness of 1st gate electrode 16a to about 50nm, the increment in wiring resistance can be controlled.

[0144] (The 9th operation gestalt) The perspective view showing MOSFET which drawing 22 requires for the 9th operation gestalt of this invention, the sectional view where that top view and drawing 23 B meet the 23B-23B line in drawing 23 A in drawing 23 A, and drawing 23 C are sectional views which meet the 23C-23C line in drawing 23 A.

[0145] With the 8th operation gestalt, 1st gate electrode 16a was formed on gate-dielectric-film 18a formed on two side faces in which a fence 13 faces mutually, and the structure of connecting these 1st gate electrode 16a mutually using 2nd gate electrode 16b formed on gate-dielectric-film (TOP insulator layer) 18b formed on the top face of a fence 13 was explained.

[0146] A \*\*\*\* 9 operation gestalt has the laminating gate electrode which consists of a gate electrode 16 formed on the gate dielectric film 18 formed in 1st gate electrode 16a on two side faces in which a fence 13 faces mutually, and three fields of that top face, and 2nd gate electrode (metal) 16b electrically connected to this gate electrode 18, as shown in drawing 22 and drawing 23 A and drawing 23 B.

[0147] In order to form such structure, after processing the gate electrode 16 into a desired configuration in the 1st operation gestalt in the process shown in drawing 8 A and drawing 8 B, the side-attachment-wall insulator layer 25 is formed in the side attachment wall of the gate electrode 16, and the source / drain field 17 is formed ( drawing 9 A, drawing 9 B). Then, an interlayer insulation film 26 is formed and flattening of this is carried out ( drawing 10 A, drawing 10 B). It is made to expose the front face of the gate electrode 16 alternatively at the time of flattening of this interlayer insulation film 26. Then, the metal cascade screen (for example, W film / TiN film / Ti film) used as 2nd gate electrode 16b is deposited, patterning is carried out to a desired configuration using the resist film (not shown), and 2nd gate electrode 16b is formed.

[0148] Also in a \*\*\*\* 9 operation gestalt, although there is possibility that will double between the gate electrode 16 and 2nd gate electrode 16b, and gap will occur like the 8th operation gestalt, it is uninfluent to the electrical property of MOSFET.

[0149] By considering as the electrode structure concerning such a \*\*\*\* 9 operation gestalt, the gate electrode 16 constituted by the Pori Si layer which doped the 1st gate electrode material, for example, an impurity, can be formed in three side faces of the both-sides side of a fence 13, and a top face. Furthermore it connects with the gate electrode 16 electrically, for example, 2nd gate electrode 16b constituted by the 2nd gate electrode material, for example, metal, and

metal cascade screen with more low resistance can be formed. For this reason, there are the features that a gate electrode material can be changed, according to the electrical property of MOSFET.

[0150] Moreover, even if it thin-film-izes the gate electrode 16 to about 50nm, the increment in wiring resistance can be controlled in the laminating metal connection layer used as the 2nd gate electrode.

[0151] (The 10th operation gestalt) Drawing 26 is the sectional view showing MOSFET concerning the 10th operation gestalt of this invention. In addition, the cross section shown in drawing 26 is equivalent to the cross section shown in drawing 1 B.

[0152] With the 1st operation gestalt, when embedding and forming the isolation insulator layer 14 in the lower boundary region of a fence 13, as shown in drawing 6 A and drawing 6 B, the isolation insulator layer 14 is formed in the extended field of the side face of a fence 13.

[0153] A \*\*\*\* 10 operation gestalt is an example to which the shape of a flush type of the isolation insulator layer 14 does not deteriorate to the lower field of a fence 13 and which is formed like so that it may have the forward tapered shape include angle theta of about 10 degrees, when embedding and forming the isolation insulator layer 14.

[0154] As shown in drawing 26, the embedding nature especially in the lower field of a fence 13 of the insulator layer 23 shown in drawing 5 A and drawing 5 B can be remarkably improved to the lower field of a fence 13 by giving the forward tapered shape include angle theta of about 10 degrees compared with the case of being perpendicular.

[0155] Moreover, what is necessary is to change etching conditions into the culmination at the time of etching of a fence 13, and just to make it the forward tapered shape include angle theta attached to it, in order to process it so that it may have cone-angle theta in the lower field of a fence 13. Giving the forward tapered shape include angle theta of about 10 degrees to the lower field of a fence 13 can be realized comparatively easily by modification of etching conditions.

[0156] Thus, by the lower field of a fence 13 having the forward tapered shape include angle theta of about 10 degrees, and making it convex Si structure with the almost perpendicular side face used as the channel of MOSFET of the up field, the embedding property of the isolation insulator layer 14 can be improved, and there are the features that the stable component isolation region can be formed.

[0157] (The 11th operation gestalt) Drawing 27 is the sectional view showing MOSFET concerning the 11th operation gestalt of this invention. In addition, the cross section shown in drawing 27 is equivalent to the cross section shown in drawing 1 B.

[0158] With the 1st operation gestalt and the 10th operation gestalt, when the isolation insulator layer 14 was embedded and formed in the lower field of a fence 13, as shown in drawing 6 A and drawing 6 B, the example currently formed so that the top face of the isolation insulator layer 14 may become almost level to the 10th page of Si substrate, and the example to which the pars-basilaris-ossis-occipitalis corner of the isolation insulator layer 14 is almost perpendicular were stated.

[0159] The example formed so that the front face of the example formed so that it may have the radius of circle whose pars-basilaris-ossis-occipitalis corner of a fence 13 is about radius =50nm so that the shape of a flush type of the isolation insulator layer 14 may not deteriorate, when embedding the isolation insulator layer 14 with a \*\*\*\* 11 operation gestalt and forming, and the isolation insulator layer 14 may not be almost level to Si substrate 10 front face and thickness may become thin toward the core of the isolation insulator layer 14 from the periphery of a fence 13 is described.

[0160] As shown in drawing 27, the embedding nature especially in the lower field of a fence 13 of the isolation insulator layer 14 shown in drawing 5 A and drawing 5 B can be remarkably improved by forming a round with a radius of about 50nm in the pars-basilaris-ossis-occipitalis corner of a fence 13.

[0161] Moreover, what is necessary is to change the etching conditions of a fence 13 and just to make it a pars-basilaris-ossis-occipitalis corner have a round, in order to process it so that the pars-basilaris-ossis-occipitalis corner of such a fence 13 may have a round.

[0162] Moreover, if the thickness of the isolation insulator layer 14 in the lower field of a fence 13 is formed so that it may become thin as it is thick in the lower field of a fence 13 and goes to the core of the isolation insulator layer 14, when processing the gate electrode 16, for example, in isolation insulator layer 14 front face of the lower circumference of a fence 13, the remainder of the gate electrode 16 can be prevented, short-circuit of gate electrode 16 can be prevented, and the yield of a product can be improved.

[0163] Moreover, what is necessary is to form the about 10nm thermal oxidation film in the side face of a fence 13, and just to embed CVD insulator layers, such as HDP (High Density Plasma) and an O<sub>3</sub>(ozone)-TEOS oxide film, through it on it, in order to process the isolation insulator layer 14 so that it may have the above-mentioned configuration. What is necessary is to adjust wet etching conditions finally, and for the direction of a CVD insulator layer to choose and

etch conditions (temperature of an etching reagent, concentration of fluoric acid, etc.) which are slow, and just to form an insulator layer from which it becomes thick thickness only near the fence 13 to the thermal oxidation film, although a CVD insulator layer is embedded and formed using the CMP method or the RIE method as shown in drawing 6 A and drawing 6 B.

[0164] Thus, by forming a round with a radius of about 50nm in the pars-basilaris-ossis-occipitalis corner of a fence, the embedding nature of the isolation insulator layer 14 especially in the lower field of a fence 13 can be improved remarkably.

[0165] Moreover, if it is [ / near the lower field of a fence 13 ] thick, and the thickness of the isolation insulator layer 14 is formed, for example so that it may become thin as it goes to the core of the isolation insulator layer 14, when processing the gate electrode 16, the remainder of the gate electrode 16 can be prevented in isolation insulator layer 14 front face of the lower part of a fence 13, short-circuit of gate electrode 16 can be prevented, and the yield of a product can be improved.

[0166] (The 12th operation gestalt) Drawing 28 is the sectional view showing MOSFET concerning the 12th operation gestalt of this invention. In addition, the cross section shown in drawing 28 is equivalent to the cross section shown in drawing 1 B.

[0167] With the 1st operation gestalt, the up corner where the top face and flat surface of a fence 13 touch stated the example mostly processed into the right angle.

[0168] A \*\*\*\* 12 operation gestalt describes rounding-off of this up corner.

[0169] As shown in drawing 28, compared with the case where an up corner is almost right-angled, the effect of the electric field from the gate electrode 16 of MOSFET can be remarkably reduced by preparing a round with a radius of about 30nm in an up corner. Thereby, pressure-proofing of gate dielectric film 18 can be improved, and the effect of the parasitism channel in concentration of gate electric field can be fallen.

[0170] There are various approaches in forming such a round with a radius of about 30nm in the up corner of a fence 13. For example, in the 1st operation gestalt, the side-attachment-wall front face of a fence 13 is oxidized thermally, leaving mask SiN film 15 in the condition which shows in drawing 6 A and drawing 6 B. Thereby, in the upper part of a fence 13, interlocking with a radius of about 30nm can be put into an up corner by [ LOCOS (Local Oxidation of Silicon) ] performing selective oxidation. Then, a round with a radius of about 30nm can be given to an up corner by removing mask SiN film 15 and forming gate dielectric film 18. The amount of a round can be somewhat changed with the amount of selective oxidation.

[0171] Thus, the thing for which a round with a radius of about 30nm is prepared in the edge corner (up corner) of the top face of a fence 13. The effect of the electric field from the gate electrode of MOSFET can be reduced remarkably, and pressure-proofing of gate dielectric film 18 can be improved, and there are the features that the effect of the parasitism channel in concentration of gate electric field can be fallen.

[0172] Moreover, as shown, for example in drawing 19, even if it exceeds 90 degrees for the include angle of the up corner of a fence 13, the same effectiveness as the above can be acquired.

[0173] (The 13th operation gestalt) The top view showing MOSFET which drawing 30 requires for the 1st example of the 13th operation gestalt of this invention, the top view showing MOSFET which drawing 31 requires for that 2nd example, and drawing 32 are the top views showing MOSFET concerning that 3rd example.

[0174] With the 5th operation gestalt, in order to realize big channel width, the fence 13 was stated about the case where two or more one MOSFETs in all are formed.

[0175] A \*\*\*\* 13 operation gestalt describes the source / drain structure in the case of using two or more fences 13 as structure with one the source / drain field 17 in all, and the gate electrode 16.

[0176] The joint structure of the source / drain field 17 in the case of having two fences 13 is shown in drawing 30 as the 1st example.

[0177] As shown in drawing 30, a fence 13 is arranged to juxtaposition and one of the two of the source / drain field 17 is communalized using fence 13 the very thing. Thereby, a fence 13 is bent superficially, is seen from a flat surface, and has "U mold" structure. The number of contacts can be reduced by taking such structure.

[0178] The joint structure of the source / drain field 17 in the case of having four fences 13 is shown in drawing 31 as the 2nd example.

[0179] As shown in drawing 31, a fence 13 is arranged to juxtaposition and every two one of the two of the source / drain field 17 is communalized using the fence itself. Thereby, the fence 13 serves as a form which saw from the flat surface and combined some "U mold" structures. The number of contacts can be reduced like the case of drawing 30 by taking such structure. Moreover, the consistency of component arrangement can be improved by changing the structure of a fence 13.



[0180] The joint structure of the source / drain field 17 in the case of having four fences 13 is shown in drawing 32 as the 3rd example.

[0181] As shown in drawing 32 , a fence 13 is arranged to juxtaposition and it has structure which combined the fence 13 of the both sides used as the source / drain field 17 using this fence 13 very thing. By taking such structure, the number of contacts can be reduced like the case of drawing 30 and drawing 31 . Moreover, the consistency of component arrangement can be improved by changing the structure of a fence.

[0182] (The 14th operation gestalt) The perspective view showing MOSFET which drawing 33 requires for the 14th operation gestalt of this invention, the sectional view where that top view and drawing 34 B meet the 34B-34B line in drawing 34 A in drawing 34 A, and drawing 34 C are sectional views which meet the 34C-34C line in drawing 34 A. Moreover, in drawing 33 and drawing 34 A - drawing 34 C, the contact and wiring which were shown in drawing 2 A are omitted, respectively.

[0183] With the 1st operation gestalt, on the outskirts, there is an isolation insulator layer 14, the channel field 15 of a fence 13 was further connected with the Si substrate 10 electrically, and the structure where substrate bias could be impressed to the channel field 15 was shown in the lower field of a fence 13.

[0184] As shown in drawing 33 and drawing 34 A - drawing 34 C, using the SOI substrate 40, on the insulator layer 41 of this SOI substrate 40, a \*\*\*\* 14 operation gestalt forms an about 200nm thin film Si layer, processes this and forms a fence 13. It is the structure where the Si layer 42 of the same conductivity type as the channel field 15 exists between insulator layers 41 still like the pars basilaris ossis occipitalis of the source / drain field 17 of MOSFET, and an insulator layer 41, for example, an embedding oxide film.

[0185] Although substrate bias cannot be impressed with such structure since it is SOI structure, the effect of degradation of its source / drain pressure-proofing etc. can be reduced by distribution being [ the effect of the stored charge (in the case of an N channel, it becomes a hole) accumulated in a channel field at the time of MOSFET actuation ] expandable to the pars basilaris ossis occipitalis of the source / drain field 17.

[0186] What is necessary is just to manufacture structure as shown in the 1st operation gestalt using the SOI substrate 40, in order to realize such structure. And it is important to form the Si layer 42 of the same conductivity type as the channel field 15 between the pars basilaris ossis occipitalis of the source / drain field 17 and an insulator layer 41.

[0187] (The 15th operation gestalt) The perspective view showing MOSFET which drawing 35 requires for the 15th operation gestalt of this invention, the sectional view where that top view and drawing 36 B meet the 36B-36B line in drawing 36 A in drawing 36 A, and drawing 36 C are sectional views which meet the 36C-36C line in drawing 36 A. Moreover, in drawing 35 and drawing 36 A - drawing 36 C, the contact and wiring which were shown in drawing 2 A are omitted, respectively.

[0188] With the 14th operation gestalt, the channel was formed in the both-sides side of a fence 13 using the SOI substrate 40, the channel was preferably depletion-ized completely at the time of actuation, and the structure of improving the short channel effect of MOSFET was stated. It is that the difference from the Fin structure MOSFET of the conventional thin film SOI ( drawing 81 ) forms the Si layer 42 of the same conductivity type as a channel between the pars basilaris ossis occipitalis of the source / drain field 17, and an insulator layer 41 at this time. Thereby, the substrate suspension effectiveness which was a problem in MOSFET using the conventional thin film SOI can be prevented.

[0189] As shown in drawing 35 and drawing 36 A - drawing 36 C, a \*\*\*\* 15 operation gestalt forms the amorphous silicon layer which has about 200nm thickness on this glass substrate 43 using a glass substrate 43, processes an amorphous silicon layer and forms MOSFET with the same fence 13 as the 14th operation gestalt. The structure where the amorphous silicon layer 44 exists by the same Si layer of a conductivity type as the channel field 15 and this example between the pars basilaris ossis occipitalis of the source / drain field 17 of MOSFET and a glass substrate 43 is the same as the 14th operation gestalt.

[0190] Although it is the amorphous silicon layer MOSFET using a glass substrate 43 by using such structure, a perfect depletion-ized channel is realizable with double-gate structure. Therefore, the property of amorphous silicon-MOSFET can be improved.

[0191] What is necessary is just to realize using the amorphous silicon layer in which the manufacture approach as shown in the 1st operation gestalt was formed on the glass substrate 43, in order to realize such structure. Of course, in a \*\*\*\* 15 operation gestalt, it is important similarly like the 14th operation gestalt to form the amorphous silicon layer 44 of the same conductivity type as the channel field 15 between the pars basilaris ossis occipitalis of the source / drain field 17 and a glass substrate 43.

[0192] (The 16th operation gestalt) Drawing 37 A - drawing 42 A and drawing 37 B - drawing 42 B are the process sectional views showing the manufacture approach of MOSFET concerning the 16th operation gestalt of this invention.

In addition, the cross section shown in drawing 37 A - drawing 42 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 37 B - drawing 42 B is equivalent to the cross section shown in drawing 2 C.

[0193] The 1st operation gestalt described the example which forms a fence 13 by etching the Si substrate 10 using the mask layer 22.

[0194] It is the approach of forming a fence 13 and forming the MOSFET structure of a double-gate mold with a perfect depletion-ized channel with a \*\*\*\* 16 operation gestalt, using an epitaxial Si layer. The approach is explained below with reference to the process sectional view shown in drawing 37 - drawing 42.

[0195] First, as shown in drawing 37 A and drawing 37 B, in forming NMOSFET in the transistor channel field of the 3 about [  $5 \times 10^{15} \text{cm}^{-3}$  high impurity concentration to ] field bearing (100) P type Si substrate 110, it forms the P type well 111 (about [ Being peak high impurity concentration. for example,  $4 \times 10^{17} \text{cm}^{-3}$  ] 3) by carrying out the ion implantation for example, of the boron ion (B+) about [ acceleration voltage 260KeV and  $2 \times 10^{13} \text{cm}^{-2}$  dose to / 2 ]. Moreover, in forming PMOSFET, it forms N well (not shown). Next, about 100nm of SiO<sub>2</sub> film 114 used as an isolation insulator layer is formed in behind all over the Si substrate 110 upper part, for example. next, the mask layer (SiN) 121 used as the Maine ingredient of the slot in the case of growing up an epitaxial Si layer -- for example, about 200nm is formed. next, the mask layer (SiO<sub>2</sub>) 122 used as the protective layer when carrying out CMP of the epitaxial Si layer -- for example, about 50nm is formed. Next, the usual resist film (not shown) and the usual RIE method are used for these cascade screens, and a desired pattern is formed in them. In this example, the slot pattern 123 for forming the fence which consists of an epitaxial Si layer is formed. Then, an etching damage, an organic substance contamination layer, etc. at the time of RIE are removed from the front face of the Si substrate 10 exposed from the slot pattern 123. This removal is performed in consideration of the epitaxial growth of Si performed at the following process, and should just be performed if needed.

[0196] Next, as shown in drawing 38 A and drawing 38 B, after removing the natural oxidation film etc. from the front face of the Si substrate 110 exposed from the slot pattern 123, epitaxial growth of the Si is carried out and the epitaxial Si layer 101 is formed. The thickness is set as thickness which fills the inside of the slot pattern 123 completely and puts it. A concrete example of the thickness is about 400nm. Next, the mask layer (SiO<sub>2</sub>) 122 is used for a mask, CMP of the front face of the epitaxial Si layer 101 is carried out, and the epitaxial Si layer 101 protruded from the slot pattern 123 on the mask layer 122 is removed. This removes the irregularity of the front face of the epitaxial Si layer 101. If it does in this way, the facet of the epitaxial Si layer 101 formed into the slot pattern 123 etc. can be removed, and the epitaxial Si layer 101 can be formed in the slot pattern 123 with a sufficient precision. It is important that it is cautious of the growth temperature in the case of epitaxial growth, an ambient atmosphere, and pretreatment, for example, a crystal defect etc. is made not to be formed in the interface of the epitaxial Si layer 101 and the Si substrate 110.

[0197] Moreover, although the mask layer (SiO<sub>2</sub>) 122 was used for the mask and CMP of the epitaxial Si layer 101 was carried out in this example, the mask layer (SiO<sub>2</sub>) 122 is also omissible by adjusting CMP conditions etc.

[0198] Next, as shown in drawing 39 A and drawing 39 B, the resist film (not shown) is used for a mask, for example, the ion implantation of the boron ion (B+) is carried out to the field in the epitaxial Si layer 101 which includes a transistor channel formation field at least, and the high concentration impurity layer 112 which has about [  $2 \times 10^{18} \text{cm}^{-3}$  - ] three high impurity concentration by peak concentration is formed in it. This high concentration impurity layer 112 functions as a punch-through stopper layer. At the time of this process, the oxide film (not shown) of about 8nm thickness is formed in epitaxial Si layer 101 front face, and the contamination to the epitaxial Si layer 101 from the resist film, for example, metal contamination etc., is prevented. Moreover, the RTA processing for about 5 minutes is used for activation of the poured-in ion in 900 degrees C and a nitrogen (N<sub>2</sub>) ambient atmosphere. The P type high concentration impurity layer 112 which has a steep profile by this can be formed. Furthermore, the resist film (not shown) is used for a mask, the impurity ion of a desired conductivity type is poured into the field which includes a transistor channel formation field, for example, and the channel impurity layer 115 is formed in it. At this time, the channel impurity layer 115 may form impurity ion only in a transistor channel field by pouring in alternatively. the case where MOSFET formed wants to set the threshold electrical potential difference (V<sub>th</sub>) as about 0.7V with an N channel mold -- for example, boron ion (B+) -- acceleration voltage, 20 KeV, an ion implantation is carried out about [  $5 \times 10^{12} \text{cm}^{-2}$  - ] two, and the channel impurity layer 115 of P type is formed in the field used as a channel so that it may become a uniform profile alternatively. This process performs an ion implantation through an oxide film (not shown). Activation of the channel impurity layer 115 may be performed by 750 degrees C and heat treatment for about 10 seconds, using next, for example, RTA, processing.

[0199] Next, as shown in drawing 40 A and drawing 40 B, the mask layer (SiO<sub>2</sub>) 122 and the above-mentioned oxide film (not shown) are removed, and the mask layer (SiN) 121 is completely removed for example, using a hot

phosphoric-acid solution. By doing in this way, the isolation insulator layer (SiO<sub>2</sub>) 114 can be saved all over a wafer by uniform thickness only around the lower field of the epitaxial Si layer 101.

[0200] Next, as shown in drawing 41 A and drawing 41 B, gate dielectric film 118 is formed in the front face of Si layer exposed to the top face which consists of an epitaxial Si layer and side face of a fence 113. Gate dielectric film 118 is formed because about 2.5nm oxidizes the front face of Si exposed, for example using an about 700-degree C radical oxidation style. In especially formation of the gate dielectric film 118 using this radical oxidation style, since it is hard to be dependent on field bearing of a side face and the unevenness on the front face of Si can realize few oxide films, an MOS transistor with few falls of channel MOBIRITI by channel interface dispersion is realizable. Moreover, since radical oxidation can form only fixed thickness at temperature with the thickness of an oxide film, it has the features that thickness variation of the oxide film during a chip in the wafer side of an oxide film can be lessened. Of course, using the oxidizing [ thermally ] method, the thermal oxidation film may usually be formed in gate dielectric film 118, and the so-called "oxy-night RAIDO film" gate dielectric film used as the SiON film may be used for it by nitriding the front face by the gas containing nitrogen.

[0201] As mentioned above with reference to drawing 25, moreover, to gate dielectric film 118 2OTa5 (tantalum oxide) film, 2Oaluminum3 film, 2OLa3 film, After using the so-called high dielectric insulator layers, such as HfO<sub>2</sub> film and ZrO<sub>2</sub> film, and forming the film of about 1nm Si oxide-film system in Si interface, for example, you may use it by making it the so-called cascade screen gate-dielectric-film structure which forms 2OTa5 film on it.

[0202] Next, as shown in drawing 42 A and drawing 42 B, deposition formation is carried out on the structure which it becomes the gate electrode 116, for example, shows the doped polycrystal Si film (about 50nm of thickness) which doped the N type impurity in drawing 41 A and drawing 41 B, on it, it becomes the gate cap film 124, for example, deposition formation of about 50nm of the SiN films is carried out. Subsequently, the resist film (not shown) is used for a mask, first, the gate cap insulator layer (SiN) 124 is etched, the gate cap insulator layer (SiN) 124 is used, and, subsequently to a mask, patterning of the doped polycrystal Si film is carried out. Thereby, the gate electrode 116 is formed. At this time, the gate electrode 116 is processed so that the level difference of a fence 113 may be straddled. For this reason, it is important to be fully able to take a ratio (selection ratio) with the etch rate of the etch rate of the gate electrode 116, and the gate dielectric film 118 and the isolation insulator layer 114, for example, to carry out patterning of the doped polycrystal Si film using conditions which have about 400. By using such etching conditions, the etching damage to the convex thin film Si layer 113 can be prevented.

[0203] Moreover, in order to reduce resistance of the gate electrode 116, it is also possible to use laminating gate electrode structure with silicide film, such as metal film, such as metal film (the TiN film, W film, aluminum film, etc. and its cascade screen) or the polycrystal Si film and W film, TiN film, aluminum film, and Cu film, and TiSi<sub>2</sub> film, instead of the doped polycrystal Si film.

[0204] Furthermore, when the ingredient of the gate electrode 116 is set to TiN etc., it is also possible by adjusting the stacking tendency etc. to adjust the threshold electrical potential difference of MOSFET using change of the work function of the gate electrode 116.

[0205] Moreover, the die length (the so-called gate length) of the gate electrode 110 is set to about 70nm. In this invention, since the short channel effect of PMOSFET can be controlled, you may design so that an N channel and the channel length with same PMOSFET may be used.

[0206] Although the following processes are not illustrated specially, as shown after drawing 9 [ of the 1st operation gestalt ] A, and drawing 9 B, the basic structure of MOSFET is completed by formation of aluminum wiring layer to formation of flattening by CMP after depositing CVD-SiO<sub>2</sub> film all over formation of the source / drain field, and a contact hole, and a pan, and completes them by deposition of the passivation film on the whole surface.

[0207] Since there is no etching damage of a side face compared with the case where can form a fence 113, can decide the width of face of the (1) fence 113 by the width of face of the slot pattern 123 using such an epitaxial Si layer 101 according to the MOSFET structure of the double-gate mold which has a perfect depletion-ized channel in the both-sides side of a fence 113 preferably, and the convex thin film Si layer 113 is formed by etching, the yield of the gate dielectric film 118 of a side face is good.

[0208] (2) Since the thickness of the isolation insulator layer 114 can be formed around the lower field of a fence 113 uniformly, the yield of isolation improves.

[0209] (3) By detaching between the isolation insulator layers 114 formed in the source / drain field, and the lower field of a convex thin film Si layer which were formed into the fence 113, the channel width of Book MOSFET is controllable by the depth of the source / drain field.

[0210] (4) By considering as a thing narrower than 0.20 micrometers, the width of face (W<sub>g</sub>) of a fence 113 can depletion-ize the channel field 115 completely with the gate electrode 116 formed in both sides. By the ability of-izing

of the channel field 115 to be carried out [ depletion ] completely, high impurity concentration of the channel field 115 can be low-concentration-ized compared with the case of the channel of a flat-surface mold. For this reason, the fall of the mobility of the carrier in the channel field 115 can be controlled. Moreover, it is hard to be influenced of fluctuation by high impurity concentration. Moreover, strong structure is realizable also to the thickness variation of gate dielectric film 118.

[0211] (5) The punch-through of MOSFET can be prevented by forming the high concentration impurity layer (punch-through stopper layer) 112 between the channel field 115 of a fence 113, and a well 111 (or Si substrate 110).

[0212] (6) In the side face of a fence 113, the punch-through between the source/drain can be prevented by realizing a configuration which is short in the up field of a fence 113, and becomes large toward a lower field about the distance between the source and a drain.

[0213] (7) Form in an extremely different configuration from the former where a part of source / drain field 117 consisted of a gate electrode 116 outside in self align, in the lower field of a fence 113. By establishing the offset structure which a part of such a gate electrode 116, and source / drain field 117 offset mutually, the punch-through in the lower field of a fence 113 can be prevented effectively.

[0214] (8) In transistor structure with a fence 113, the so-called high dielectric insulator layers, such as  $2\text{OTa5}$  film, can be used for gate dielectric film 118. And since it is the structure where the gate electrode 116 has transistor structure in the both sides of a side face with convex, the cut-off characteristic of a transistor can be improved more effectively.

[0215] (The 17th operation gestalt) Drawing 43 A - drawing 47 A and drawing 43 B - drawing 47 B are the process sectional views showing the manufacture approach of MOSFET concerning the 17th operation gestalt of this invention. In addition, the cross section shown in drawing 43 A - drawing 47 A is equivalent to the cross section shown in drawing 2 B, and the cross section shown in drawing 43 B - drawing 47 B is equivalent to the cross section shown in drawing 2 C.

[0216] The 16th operation gestalt explained the manufacture approach of having formed the convex thin film Si layer 113, and forming the MOSFET structure of a double-gate mold with a perfect depletion-ized channel using the epitaxial Si layer 101.

[0217] With a \*\*\*\* 17 operation gestalt, although a fence 113 is formed using the epitaxial Si layer 101, how to form gate-dielectric-film 118b of different thickness from the side face in the top face of the fence 113 is stated.

[0218] First, as shown in drawing 43 A and 43B, in forming NMOSFET in the transistor channel field of the 3 about [  $5 \times 10^{15} \text{cm}^{-3}$  high impurity concentration to ] field bearing (100) P type Si substrate 110, it forms the P type well 111 (about [ Being peak high impurity concentration. for example, /  $4 \times 10^{17} \text{cm}^{-3}$  - ] 3) by carrying out the ion implantation for example, of the boron ion ( $\text{B}^+$ ) about [ acceleration voltage  $260 \text{KeV}$  and  $2 \times 10^{13} \text{cm}^{-2}$  dose to / 2 ]. Moreover, in forming PMOSFET, it forms N well (not shown). Next, about  $100 \text{nm}$  of  $\text{SiO}_2$  film 114 used as an isolation insulator layer is formed in behind all over the Si substrate 110 upper part, for example. next, the mask layer ( $\text{SiN}$ ) 121 used as the Maine ingredient of the slot in the case of growing up an epitaxial Si layer -- for example, about  $250 \text{nm}$  is formed. Next, the usual resist film (not shown) and the usual RIE method are used for these cascade screens, and a desired pattern is formed in them. In this example, the slot pattern 123 for forming the fence which consists of an epitaxial Si layer is formed. Then, in consideration of the epitaxial growth of Si performed at the following process, the process which removes an etching damage, an organic substance contamination layer, etc. at the time of RIE may be performed from the front face of the Si substrate 10 exposed from the slot pattern 123. Next, after removing the natural oxidation film etc. from the front face of the Si substrate 110 exposed from the slot pattern 123, epitaxial growth of the Si is carried out and the epitaxial Si layer 101 is formed. The thickness is set as thickness which fills the inside of the slot pattern 123 completely and puts it. A concrete example of the thickness is about  $400 \text{nm}$ . Next, CMP of the front face of the epitaxial Si layer 101 is carried out, and the epitaxial Si layer overflowing from a slot is removed. This removes the irregularity of the front face of the epitaxial Si layer 101. If it does in this way, the facet of the epitaxial Si layer 101 formed into the slot pattern 123 etc. can be removed, and the epitaxial Si layer 101 can be formed in the slot pattern 123 with a sufficient precision. It is important that it is cautious of the growth temperature in the case of epitaxial growth, an ambient atmosphere, and pretreatment, for example, a crystal defect etc. is made not to be formed in the interface of the epitaxial Si layer 101 and the Si substrate 110.

[0219] Next, as shown in drawing 44 A and drawing 44 B, about  $20 \text{nm}$  gate-dielectric-film (TOP insulator layer) 118b is formed in epitaxial Si layer 101 exposed front face, for example. If the oxidizing [ thermally ] method is used at this time, gate-dielectric-film (TOP insulator layer) 118b can be alternatively formed only in the front face of the exposed epitaxial Si layer 101 from there being a mask layer ( $\text{SiN}$ ) 121.

[0220] Next, as shown in drawing 45 A and drawing 45 B, the resist film (not shown) is used for a mask, for example, the ion implantation of the boron ion ( $\text{B}^+$ ) is carried out to the field in the epitaxial Si layer 101 which includes a

transistor channel formation field at least, and the high concentration impurity layer 112 which has about  $[8 \times 10^{17} \text{cm}^{-3}]$  three high impurity concentration by peak concentration is formed in it. This high concentration impurity layer 112 functions as a punch-through stopper layer. The RTA processing for about 5 minutes is used for activation of the ion poured in at this time in 900 degrees C and a nitrogen (N<sub>2</sub>) ambient atmosphere. The P type high concentration impurity layer 112 which has a steep profile by this is formed. Furthermore, the resist film (not shown) is used for a mask, the impurity ion of a desired conductivity type is poured into the field which includes a transistor channel formation field, for example, and the channel impurity layer 115 is formed in it. At this time, the channel impurity layer 115 may form impurity ion only in a transistor channel field by pouring in alternatively. the case where MOSFET formed wants to set the threshold electrical potential difference (V<sub>th</sub>) as about 0.4V with an N channel mold -- for example, boron ion (B<sup>+</sup>) -- acceleration voltage, 20 KeV, an ion implantation is carried out about  $[3 \times 10^{12} \text{cm}^{-2}]$  two, and the channel impurity layer 115 of P type is formed in the field used as a channel so that it may become a uniform profile alternatively. Activation of the channel impurity layer 115 may be performed by 750 degrees C and heat treatment for about 10 seconds, using next, for example, RTA, processing.

[0221] In addition, this example showed the example which performs the ion implantation for obtaining the channel impurity layer 115 of P type through gate-dielectric-film (TOP insulator layer) 118b. However, after forming the sacrifice oxide film of about 8nm thickness in the front face of the epitaxial Si layer 101 and performing an ion implantation through this sacrifice oxide film first, this sacrifice oxide film is exfoliated and gate-dielectric-film (TOP insulator layer) 118b may newly be formed in the front face of the epitaxial Si layer 101. Thus, by performing the ion implantation through a sacrifice oxide film, the metal contamination to the epitaxial Si layer 101 from the resist film when using the resist film as a mask and performing an ion implantation etc. can be prevented.

[0222] Next, as shown in drawing 46 A and drawing 46 B, the mask layer (SiN) 121 is completely removed for example, using a hot phosphoric-acid solution. By doing in this way, the isolation insulator layer (SiO<sub>2</sub>) 114 can be saved all over a wafer by uniform thickness only around the lower field of the epitaxial Si layer 101. Next, gate dielectric film 118 is formed in the front face of Si layer exposed to the top face which consists of an epitaxial Si layer and side face of a fence 113. Gate dielectric film 118 is formed because about 2.5nm oxidizes the front face of Si exposed, for example using an about 700-degree C radical oxidation style. In especially formation of the gate dielectric film 118 using this radical oxidation style, since it is hard to be dependent on field bearing of a side face and the unevenness on the front face of Si can realize few oxide films, an MOS transistor with few falls of channel MOBIRITI by channel interface dispersion is realizable. Moreover, since radical oxidation can form only fixed thickness at temperature with the thickness of an oxide film, it has the features that thickness variation of the oxide film during a chip in the wafer side of an oxide film can be lessened. Of course, using the oxidizing [ thermally ] method, the thermal oxidation film may usually be formed in gate dielectric film 118, and the so-called "oxy-night RAIDO film" gate dielectric film used as the SiON film may be used for it by nitriding the front face by the gas containing nitrogen.

[0223] Moreover, as mentioned above with reference to drawing 25, after using the so-called high dielectric insulator layers, such as 2OTa5 (tantalum oxide) film, HfO<sub>2</sub> film, and ZrO<sub>2</sub> film, and forming the film of about 1nm Si oxide-film system in Si interface, for example, you may use it for gate dielectric film 118 in the so-called cascade screen gate-dielectric-film structure which forms 2OTa5 film on it, carrying out.

[0224] Next, as shown in drawing 47 A and drawing 47 B, deposition formation is carried out on the structure which it becomes the gate electrode 116, for example, shows the doped polycrystal Si film (about 80nm of thickness) which doped the N type impurity in drawing 41 A and drawing 41 B, on it, it becomes the gate cap film 124, for example, deposition formation of about 50nm of the SiN films is carried out. Subsequently, the resist film (not shown) is used for a mask, first, the gate cap insulator layer (SiN) 124 is etched, the gate cap insulator layer (SiN) 124 is used, and, subsequently to a mask, patterning of the doped polycrystal Si film is carried out. Thereby, the gate electrode 116 is formed. At this time, the gate electrode 116 is processed so that the level difference of a fence 113 may be straddled. For this reason, it is important to be fully able to take a ratio (selection ratio) with the etch rate of the etch rate of the gate electrode 116, and the gate dielectric film 118 and the isolation insulator layer 114, for example, to carry out patterning of the doped polycrystal Si film using conditions which have about 400. The etching damage to a fence 113 can be prevented by using such etching conditions.

[0225] Moreover, in order to reduce resistance of the gate electrode 16, it is also possible to use laminating gate electrode structure with silicide film, such as metal film, such as metal film (the TiN film, W film, aluminum film, etc. and its cascade screen) or the polycrystal Si film and W film, TiN film, aluminum film, and Cu film, and TiSi<sub>2</sub> film, instead of the doped polycrystal Si film.

[0226] Furthermore, when the ingredient of the gate electrode 16 is set to TiN etc., it is also possible by adjusting the stacking tendency etc. to adjust the threshold electrical potential difference of MOSFET using change of the work



function of the gate electrode 16.

[0227] Moreover, the die length (the so-called gate length) of the gate electrode 16 is set to about 50-70nm. In this invention, although mentioned later in detail, since the short channel effect of PMOSFET can be controlled, you may design so that an N channel and the channel length with same PMOSFET may be used.

[0228] By using such structure, since the thickness of gate-dielectric-film (TOP insulator layer) 118b formed in the top face is thicker than the thickness of gate-dielectric-film 118a formed in the both-sides side in the channel field 115 of the 3rd page (a top face, both-sides side) of a fence 113, the effect of the gate electric-field concentration in an up corner can be reduced. Therefore, fluctuation of the threshold electrical potential difference when being able to set it as the value of a request of a threshold electrical potential difference with high precision, and impressing a substrate bias property, i.e., substrate bias, can be controlled.

[0229] (The 18th operation gestalt) The top view showing complementary MOS FET which drawing 48 A requires for the 18th operation gestalt of this invention, the sectional view where drawing 48 B meets the 48B-48B line in drawing 48 A, the sectional view where drawing 48 C meets the 48C-48C line in drawing 48 A, and drawing 48 D are the sectional views in alignment with the 48D-48 D line in drawing 48 A.

[0230] Hereafter, the 18th operation gestalt is explained with the manufacture approach.

[0231] Drawing 49 - drawing 54 are the process sectional views showing complementary MOS FET concerning the 18th operation gestalt for every main production processes, respectively. In addition, the cross section shown in drawing 49 - drawing 54 is equivalent to the cross section shown in drawing 48 B.

[0232] As shown in drawing 49, first, the 3 about [  $5 \times 10^{15} \text{cm}^{-3}$  high impurity concentration to ] field bearing (100) P type Si substrate 310, The resist film (not shown) is used for a mask to a NMOSFET formation field (NMOSFET field). For example, the ion implantation of the boron ion (B<sup>+</sup>) is carried out about [ acceleration voltage 200KeV and  $2 \times 10^{13} \text{cm}^{-2}$  dose to / 2 ], and P type well 311p (about [ Being peak high impurity concentration. for example, /  $4 \times 10^{17} \text{cm}^{-3}$  ] 3) is formed.

[0233] Next, the resist film (not shown) is used for a mask, for example, the ion implantation of the boron ion (B<sup>+</sup>) is carried out to the field in P type well 311p which includes the transistor channel formation field of an N channel at least, and P type high concentration impurity layer 312p which has about [  $8 \times 10^{17} \text{cm}^{-3}$  ] three high impurity concentration by peak concentration is formed in it. P type high concentration impurity layer 312p functions as a punch-through stopper layer.

[0234] Next, the resist film (not shown) is used for a mask, for example, the ion implantation of the phosphorus ion (P<sup>+</sup>) is carried out to the PMOSFET formation field (PMOSFET field) of the P type Si substrate 310 about [ acceleration voltage 600KeV and  $2.5 \times 10^{13} \text{cm}^{-2}$  dose to / 2 ], and N type well 311n (about [ Being peak high impurity concentration. for example, /  $5 \times 10^{17} \text{cm}^{-3}$  ] 3) is formed in it.

[0235] Next, 312n of N type high concentration impurity layers which use the resist film (not shown) for a mask, for example, carry out the ion implantation of the phosphorus ion (P<sup>+</sup>) to the field in N type well 311n which includes the transistor channel formation field of a P channel at least about [ acceleration voltage 130KeV and  $2 \times 10^{13} \text{cm}^{-2}$  dose to / 2 ], and have about [  $9 \times 10^{17} \text{cm}^{-3}$  ] three high impurity concentration in it by peak concentration is formed. 312n of N type high concentration impurity layers functions as a punch-through stopper layer.

[0236] The oxide film (not shown) of about 8nm thickness is formed in the front face of the P type Si substrate 310 at the time of a these ion grouting degree. Thus, the contamination, for example, metal contamination, to the P type Si substrate 310 from the resist film (not shown) is prevented. Moreover, the RTA processing for about 5 minutes is used for activation of the poured-in ion in 900 degrees C and a nitrogen (N<sub>2</sub>) ambient atmosphere. The high concentration impurity layers 312p and 312n which have a steep profile by this can be formed.

[0237] Furthermore, the epitaxial Si layer 301 with about [  $10^{15} \text{cm}^{-3}$  ] three high impurity concentration is formed in the whole surface about 200nm of thickness with P type.

[0238] Furthermore, the resist film (not shown) is used for a mask, the impurity ion of a desired conductivity type is poured into the field which includes a transistor, a P type channel formation field, and an N type channel formation field, for example, and 315n of N type channel impurity layers and P type channel impurity layer 315p are formed in it. At this time, 315n of these channel impurity layers and P type channel impurity layer 315p may form impurity ion only in a transistor, a P type channel formation field, and an N type channel formation field by pouring in alternatively, respectively. By this example, the latter is adopted and LOCAL channel field (P type layer) 315p alternatively formed in the cross section shown in drawing 49, respectively and 315n (N type layer) of LOCAL channel fields are shown.

[0239] With an N channel mold, when MOSFET formed wants to set the threshold electrical potential difference (V<sub>th</sub>) as about 0.4V, it carries out the ion implantation for example, of the boron fluoride ion (BF<sub>2</sub><sup>+</sup>) about [  $3 \times 10^{12} \text{cm}^{-2}$  ] two 15 KeV, and it forms P type LOCAL channel field 315p in the field used as a channel so that it may become a

uniform profile alternatively.

[0240] Similarly, with a P channel mold, when MOSFET formed wants to set the threshold electrical potential difference ( $V_{th}$ ) as about -0.4V, it carries out the ion implantation for example, of the phosphorus ion (P+) about [ acceleration voltage 100KeV and  $2 \times 10^{13} \text{cm}^{-2}$  dose to / 2 ], and it forms 315n of N type LOCAL channel fields in the field used as a channel so that it may become a uniform profile alternatively. These processes perform an ion implantation through an oxide film (not shown). Activation of these channel fields 315p and 315n may be performed by 750 degrees C and heat treatment for about 10 seconds, using next, for example, RTA, processing.

[0241] next, the above-mentioned oxide film (not shown) -- removing -- again -- the whole surface -- the mask layer (SiO two-layer) 322 of the thickness of 321 or about 20nm of mask layer (SiN) film of the thickness of 320 or about 20nm of SiO two-layer of about 5nm thickness -- forming -- the lithography method and the RIE method -- using -- a desired configuration, for example, NMOSFET, and PMOSFET -- the configuration used as each component field is processed. The dotted line in drawing 49 shows the field by which etching removal is carried out at a next process.

[0242] Next, as shown in drawing 50, the mask layer 322 is used for an etching mask, the structure shown in drawing 49 is etched, and the fences 313p and 313n used as the source, a drain, and a channel are formed, respectively. These fences [ 313p and 313n ] height is about 250nm, respectively. Thus, a slot with a depth of about 250nm is formed by etching the structure shown in drawing 49, for example using the RIE method until it reaches a part of P type well 311p in the Si substrate 310, and an N type well 311n part. Thereby, Fences 313p and 313n are formed, respectively. Next, while cleaning the bottom of a Fences [ 313p and 313n ] side face or a slot using ashing, wet processing, etc., Si layer which received the damage by RIE is removed. Thereby, Si front face with few damages is exposed at the bottom of a Fences [ 313p and 313n ] side face or a slot. Next, an oxide film (not shown) is formed in the bottom of a Fences [ 313p and 313n ] side face or a slot in order to improve an interface property. It is desirable to use for formation of this oxide film the radical oxidation style using an oxygen radical which can form a good oxide film at low temperature (for example, about 700 degrees C). Thus, the oxide film (not shown) of about 7nm thickness is formed in the bottom of a Fences [ 313p and 313n ] side face or a slot using a radical oxidation style.

[0243] next, said oxide film -- minding -- a slot -- an insulator layer 2, for example, SiO, -- desirable -- TEOS-SiO two-layer -- it embeds by 323. This forms the so-called trench mold isolation (STI). this -- the whole surface -- about 500nm TEOS-SiO two-layer -- an about 700 degrees C [ after carrying out deposition formation of 323 using a CVD method with a membrane formation temperature of about 650 degrees C ] radical oxidizing atmosphere -- TEOS-SiO two-layer -- 323 -- a CVD oxide film -- densifying . then, the CMP method -- using -- TEOS-SiO two-layer -- flattening of the front face of 323 is carried out. this time -- up to the front face of SiN film 321 -- TEOS-SiO two-layer -- 323 is embedded. thereby -- a slot -- TEOS-SiO two-layer -- it is evenly embedded by 323.

[0244] next, it is shown in drawing 51 -- as -- TEOS-SiO two-layer -- the isolation insulator layer 314 for isolation used as about 100nm thickness is formed in the pars basilaris ossis occipitalis of a slot by carrying out etchback of 323 for example, using the RIE method.

[0245] Next, as shown in drawing 52, wet removal of the mask layer (SiN) 321 is carried out using hot phosphoric acid etc. Subsequently, the oxide film (not shown) currently formed in the side face of a slot and SiO two-layer 320 are exfoliated using the solution of a fluoric acid system, and Si front face is exposed from a Fences [ 313p and 313n ] top face and its side face. Subsequently, an about 700-degree C radical oxidation style is used for the front face of exposed Si, and the gate dielectric film 318 of about 2.5nm thickness is formed in it. In especially formation of the gate dielectric film 318 using this radical oxidation style, since it is hard to be dependent on field bearing of a side face and the unevenness on the front face of Si can realize few oxide films, an MOS transistor with few falls of channel MOBIRITI by channel interface dispersion is realizable. Moreover, since radical oxidation can form only fixed thickness at temperature with the thickness of an oxide film, it has the features that thickness variation of the oxide film during a chip in the wafer side of an oxide film can be lessened. Of course, using the oxidizing [ thermally ] method, the thermal oxidation film may usually be formed in gate dielectric film 318, and the so-called "oxy-night RAIDO film" gate dielectric film used as the SiON film may be used for it by nitriding the front face by the gas containing nitrogen.

[0246] Furthermore, as shown in drawing 25, the so-called high dielectric insulator layers (high-kappa film), such as not only SiO<sub>2</sub> film but 2OTa<sub>5</sub> (tantalum oxide) film, and HfO<sub>2</sub> film, ZrO<sub>2</sub> film, may be used for gate dielectric film 18. Moreover, when 2OTa<sub>5</sub> film is used, in order to reduce an interface-state-density consistency with Si interface, for example, after forming the film of about 1nm Si oxide-film system in Si interface, you may use it by making it the so-called cascade screen gate-dielectric-film structure which forms 2OTa<sub>5</sub> film on it.

[0247] Next, as shown in drawing 53, deposition formation is carried out on the structure which it becomes the gate electrode 316, for example, shows the doped polycrystal Si film (about 50nm of thickness) with which the N type

impurity was doped in drawing 52, on it, it becomes the gate cap insulator layer 324, for example, deposition formation of about 100nm of the SiN films is carried out. Subsequently, the resist film (not shown) is used for a mask, first, the gate cap insulator layer (SiN) 324 is etched, the gate cap insulator layer (SiN) 324 is used, and, subsequently to a mask, patterning of the doped polycrystal Si film is carried out. Thereby, the gate electrode 316 is formed. At this time, the gate-electrode 316 is processed so that the level difference of a fence 313 may be straddled. For this reason, it is important to be fully able to take the ratio (selection ratio) of the etch rate of the gate electrode 316 and the etch rate of gate dielectric film 318, for example, to carry out patterning of the doped polycrystal Si film using conditions which have about 400. By using such etching conditions, fence 313p and the etching damage through which it passes 313n, respectively can be prevented. Moreover, in order to reduce resistance of the gate electrode 316, it is also possible to use laminating gate electrode structure with silicide film, such as metal film, such as metal film (the TiN film, W film, aluminum film, etc. and its cascade screen) or the polycrystal Si film and W film, TiN film, aluminum film, and Cu film, and TiSi<sub>2</sub> film, instead of the doped polycrystal Si film. Furthermore, when the ingredient of the gate electrode 316 is set to TiN etc., it is also possible by adjusting the stacking tendency etc. to adjust the threshold electrical potential difference of MOSFET using change of the work function of the gate electrode 16.

[0248] In the case of CMOS structure, to an N channel, it is also possible still like this example to use a P+ mold polycrystal Si layer gate electrode for an N+ mold polycrystal Si layer gate electrode and a P channel as an electrode volume phase.

[0249] Moreover, the die length (the so-called gate length) of the gate electrode 316 is set to about 70nm. Since the short channel effect of PMOSFET can be controlled in this invention, it is also possible to design so that an N channel and the channel length with same PMOSFET may be used.

[0250] Next, as shown in drawing 54, the P type source / drain field 317p, and 317n of the N type sources / drain fields are formed, respectively with the ion-implantation which used the resist film (not shown), the gate cap insulator layer 324, and the gate electrode 316 for the mask. in order to ease the side attachment wall of the gate electrode 316, and electric-field concentration of a pars-basilaris-ossis-occipitalis corner at this time -- the gate electrode 316 -- for example, RTO of a radical oxidation style or low temperature -- the oxide film (not shown) which oxidizes using law etc., for example, has about 2nm thickness may be formed.

[0251] Moreover, depth (X<sub>j</sub>) control of the source / drain fields 317p and 317n is an important process which determines the channel width of a convex Si transistor. Cautions are especially required for a temperature setup of heat treatment including activation of the source / drain fields [ 317p and 317n ] impurity etc.

[0252] In this example for this reason, first, after carrying out \*\*\*\* formation of the gate electrode 316 for N-mold diffusion layer 317na and P-mold diffusion layer 317pa for masks, an insulator layer (SiO<sub>2</sub> film and SiN film) is deposited on the whole surface with a CVD method. Moreover, the ion notes entry condition at the time of forming N-mold diffusion layer 317na is about [ acceleration voltage 40KeV and 4x10<sup>13</sup>cm dose to / 2 ] about impregnation of for example, phosphorus ion (P+). Of course, the ion implantation of the arsenic ion (As) etc. may be carried out. Then, RIE of the whole surface is carried out and the side-attachment-wall insulator layer 325 is formed in the side attachment wall of gate electrode 316 pattern, and a Fences [ 313p and 313n ] side attachment wall. Then, the ion implantation of the arsenic (As+) ion is carried out about [ acceleration voltage 20KeV and 5x10<sup>15</sup>cm dose to / 2 ], the N type source / drain field (N+ mold diffusion layer) 317nb is formed, for example, fluoride book RN (BF<sub>2</sub>+) ion is poured in further, and the P type source / drain field (P+ mold diffusion layer) 317nb is formed. The source / drain fields 317p and 317n which had the so-called gate extension structure as shown in drawing 29 D by this are formed, respectively. It is also possible to consider as the single source / drain structure, of course.

[0253] The depth (W<sub>n</sub>) of the N type source / 317n of drain fields and the depth (W<sub>p</sub>) of the P type source / drain field 317p are controlled by the thermal activation after the final ion-implantation stratification, or heat treatment conditions. For example, each ion notes entry condition (acceleration voltage and dose) and thermal activation conditions are controlled, and it realizes so that it may become about [ of N type ] junction depth (W<sub>n</sub>) = 0.15micrometer, and so that it may become about [ of P type ] junction depth (W<sub>p</sub>): 0.20micrometer.

[0254] moreover -- the case where it is made lower than for example, <50microomegacm extent when it is necessary to reduce the specific resistance of the source / drain fields 317n and 317p -- the front face of the source / drain fields 317n and 317p -- TiSi<sub>2</sub>, CoSi<sub>2</sub>, PtSi, and Pd<sub>2</sub> -- silicide layers (not shown), such as Si, IrSi<sub>3</sub>, and RhSi, may be formed. In the P type source / drain field 317p, Pd<sub>2</sub>Si is especially effective.

[0255] In this example, the offset-field used as the gate electrode 316 and offset will exist in each lower part of the P type source / drain field 317p of a lower part [ of the N type source / 317n of drain fields of the side face of fence 313p ], and fence 313n side face. This is because the source / drain fields 317n and 317p are formed by the ion-implantation and thermal diffusion from a front face. It has the structure where the punch-through in the lower field of



the source / drain fields 317n and 317p can be prevented, by existence of this offset field and the ion-implantation layer for punch-through prevention (punch-through stopper layer 312).

[0256] further -- this example -- Fences 313n and 313p -- the time of an ion implantation to form the source / drain fields 317n and 317p, since each side face is covered with the side-attachment-wall insulator layer 325 -- Fences 313n and 313p -- the ion implantation to each top face becomes main, and the ion implantation of the impurity to a side face has structure which can be prevented.

[0257] Next, as shown in drawing 48 A - drawing 48 D, using a CVD method, on the structure shown in drawing 54, SiO<sub>2</sub> [ about 500nm ] is deposited, for example, and an interlayer insulation film 326 is formed. Then, it is an about 700-degree C radical oxidizing atmosphere, for example, an interlayer insulation film 326 is densified about 30 minutes. Like this heat process, you may carry out to serve also as activation of the ion-implantation layer of the source / drain fields 317n and 317p. Temperature of densifying is low-temperature-ized or RTA processing of msec (ms) extent may be performed at about 850 degrees C to control the depth (Wn, Wp) of these sources / drain fields 317n and 317p. Furthermore these may be used together and the ion-implantation layer of the source / drain fields 317n and 317p may be activated. Then, using the CMP method, flattening of the interlayer insulation film 326 is carried out, and flattening of the component front face is carried out. Next, using the resist film (not shown) and the RIE method, a contact hole 327 is formed, W (tungsten) film, aluminum (aluminum) film, TiN (titanium nitride) film / Ti (titanium) film, and those cascade screens are embedded in the contact hole 327, and the contact plug 328 is formed. Furthermore, the aluminum wiring layer 329 is formed. By furthermore depositing the passivation film (not shown) on the whole surface, the basic structure of complementary MOS FET concerning the 18th operation gestalt of this invention is completed.

[0258] Thus, this invention is applicable also to complementary MOS FET. Thereby, various CMOS circuits can be constituted a CMOS inverter circuit and by changing wiring.

[0259] Moreover, as especially shown in drawing 48 A - drawing 48 D, although a superficial design area is the same at NMOSFET and PMOSFET, the depth (Wn) of the N type source / 317n of drain fields differs from the depth (Wp) of the P type source / drain field 317p. This shows that the MOSFET with the same superficial design area from which the channel width of a P channel of an N channel differs is [ but ] realizable.

[0260] When a CMOS circuit was designed conventionally, compared with NMOSFET, a superficial design area of PMOSFET was designed twice [ about ]. It is for controlling the variation in the drive capacity resulting from the difference of electronic mobility and the mobility of an electron hole.

[0261] However, if CMOS with the fence concerning this invention is used, since channel width is changeable using the difference of Wn and Wp, the difference of the flat-surface area of NMOSFET and the flat-surface area of PMOSFET is reducible. This is the big features of a \*\*\*\* 18 operation gestalt.

[0262] Also in a \*\*\*\* 18 operation gestalt, (1) fences [ 313p and 313n ] width of face (Wg) can be depletion-ized by making it narrower than 0.20 micrometers completely [ P type LOCAL channel field 315p and 315n of both N type LOCAL channel fields ] with the gate electrode 316 formed in the these fences [ 313p and 313n ] both-sides side. These channel fields [ 315p and 315n ] high impurity concentration can be low-concentration-ized compared with the case of the channel of a flat-surface mold, respectively by the ability of-izing of the 315n to be carried out [ these channel field 315p and / depletion ] completely. For this reason, the fall of the mobility of the carrier in these channel fields 315p and 315n can be controlled. Moreover, it is hard to be influenced of fluctuation by high impurity concentration. Moreover, strong structure is realizable also to the thickness variation of gate dielectric film 318.

[0263] (2) The punch-through of MOSFET can be prevented by forming the high concentration impurity layer (punch-through stopper layer) 312 between the Fences [ 313p and 313n ] channel fields 315p and 315n and Wells 311p and 311n (or Si substrate 310).

[0264] (3) Form in an extremely different configuration from the former where the source / drain fields [ 317p and 317n ] part consisted of a gate electrode 316 outside in self align, in a Fences [ 313p and 313n ] lower field. The punch-through in a Fences [ 313p and 313n ] lower field can be effectively prevented by establishing the offset structure which such a gate electrode 316 and the source / drain fields [ 317p and 317n ] part offset mutually.

[0265] (4) When forming contact in Fences [ 313p and 313n ] the source / drain fields 317p and 317n, contact can be formed not only using a convex thin film Si layers [ 313p and 313n ] top face but using a part of those side faces. The fences 313p and 313n used as the source / drain fields 317p and 317n are because it is time [ what ] deep compared with the depth of the source / drain field with the same conventional gate length of MOSFET. The contact resistance by detailed MOSFET can be reduced according to the contact structure of such the source/DOREINHE.

[0266] (5) In transistor structure with Fences 313p and 313n, the source / drain fields 317p and 317n may be made not only into the single source / drain structure but into structure with the so-called LDD high concentration source / drain

field 317pb, 317nb, and the low concentration source / drain field 317pa and 317na. If it does in this way, the source / drain field 317p, and about 317n electric field can be eased, and the dependability of MOSFET can be improved.

[0267] (6) When forming a CMOS circuit using NMOSFET formed in fence 313p, and PMOSFET formed in 313n of convex thin film Si layers, change the depth (Wp) of the P type source / drain field 317p, and the depth (Wn) of the N type source / 317n of drain fields. The difference of the superficial design dimension of PMOSFET and NMOSFET resulting from the difference between electronic mobility and the mobility of an electron hole can be contracted by changing Wp and Wn.

[0268] Specifically, the depth (Wp) of the P type source / drain field 317p is made deeper than the depth (Wn) of the N type source / 317n of drain fields. Thereby, even if the superficial design dimension is mutually the same, it can make channel width of PMOSFET larger than the channel width of NMOSFET. Thereby, when a CMOS circuit is designed, the area of PMOSFET can be reduced and the whole circuit area can be reduced.

[0269] (7) Using MOSFET formed in Fences 313p and 313n, change mutually the depth of the P type source / drain field 317p, and change mutually the depth of the N type source / 317n of drain fields. Thereby, the MOSFET with the same superficial design dimension from which channel width differs is [ but ] realizable. By doing in this way, when a circuit is designed, the area of MOSFET can be reduced, and the whole circuit area can be reduced.

[0270] (The 19th operation gestalt) The top view showing complementary MOS FET which drawing 55 A requires for the 19th operation gestalt of this invention, the sectional view where drawing 55 B meets the 55B-55B line in drawing 55 A, and drawing 55 C are sectional views which meet the 55C-55C line in drawing 55 A.

[0271] The 18th operation gestalt showed the case where the depth Wn of the N type source / 317n of drain fields of NMOSFET and the depth Wp of the P type source / drain field 317p of PMOSFET were changed mutually.

[0272] a \*\*\*\* 19 operation gestalt -- two or more NMOSFET(s) -- each N type source / drain field 317n-1, 317n-2 and -- the depth Wn1 and Wn2 of 317 n-n, -- Wnn, and two or more PMOSFET(s) -- each P type source / drain field 317p-1, 317p-2 and -- it is the case where the depth Wp1 and Wp2 of 317 p-n and -- Wpn are changed mutually.

[0273] In drawing 55 A - drawing 55 C, although the case of the two different source / drain field depth (it is equivalent to channel width) is shown, respectively, it is clear that it can apply when it has two or more depths of n pieces.

[0274] Thus, the degree of freedom which designs NMOSFET with different channel width and PMOSFET increases by realizing channel width of two or more N channels and a P channel. Namely, it can choose now from a design-or manufacture-point whether it realizes whether the number of Fences 313n or 313p realizes two or more channel width with two or more channel width like a \*\*\*\* 19 operation gestalt. This is the big features of this operation gestalt.

[0275] (The 20th operation gestalt) Drawing 56 is the sectional view showing a DRAM memory cell with the trench mold capacitor structure concerning the 20th operation gestalt of this invention. In addition, the field surrounded by the dotted line corresponds to a 1-bit DRAM memory cell among drawing 56.

[0276] A \*\*\*\* 20 operation gestalt is the example which used MOSFET explained for example, with the 1st operation gestalt for the transfer transistor which connects mutually the trench mold capacitor and bit line of a DRAM memory cell.

[0277] As shown in drawing 56, the source / drain field is electrically connected with the are recording electrode of a capacitor on the up side face of a trench. With the structure of the conventional flat-surface mold MOSFET, this side-attachment-wall contact field became the source/drain deep to a vertical mold, and had checked the source / drain thin film-ization of the flat-surface mold MOSFET.

[0278] If MOSFET concerning this invention is used like a \*\*\*\* 20 operation gestalt, even if the diffusion layer from side-attachment-wall contact affects it to the source / drain field of MOSFET and the depth of the source/drain becomes deep, the effect can fully be controlled with the gate electrode formed in the side attachment wall convex [ Si ]. That is, it has structure which can control the short channel effect by the elongation of the diffusion layer from side-attachment-wall contact. In order to realize a passage word line at this time, the first gate electrode including the usual side attachment wall is formed by the Pori Si layer, and its structure connected with second another gate electrode is [ the first gate electrode and passage word line ] desirable. It is more desirable to embed the first gate inter-electrode by the insulator layer, and to make it form furthermore. By doing in this way, the MOSFET structure using a fence is applicable to the transistor of DRAM.

[0279] (The 21st operation gestalt) Drawing 57 is the sectional view showing a DRAM memory cell with the stack mold capacitor structure concerning the 21st operation gestalt of this invention. In addition, the field surrounded by the dotted line corresponds to a 1-bit DRAM memory cell among drawing 57.

[0280] A \*\*\*\* 21 operation gestalt is the example which used MOSFET explained for example, with the 1st operation gestalt for the transfer transistor which connects mutually the stack mold capacitor and bit line of a DRAM memory cell.

[0281] As shown in drawing 57, it is the description that bit line contact and are recording electrode contact are lifted and formed in the upper part of a gate electrode in this example using Pori Si. It was difficult to fully reduce contact resistance in a detailed contact field in the structure of the conventional flat-surface mold MOSFET. If the convex Si structure MOSFET of this example is used, since contact can use and form not only the flat-surface section but a lateral portion, contact resistance can be reduced. Moreover, in the case of the stack capacitor using high dielectric insulator layers, such as 2OTa5 film, and BST film, STO film, after forming MOSFET, capacitor formation was performed, but the source / drain field depth of MOSFET were extended at the elevated-temperature processes at that time (crystallization annealing of about 750 degrees etc.), and there was a problem in which the short channel effect occurs.

[0282] With the MOSFET structure of a \*\*\*\* 21 operation gestalt, the short channel effect can fully be controlled. That is, it has structure which can control the short channel effect by the elongation of the source / drain field in a capacitor formation process. In order to realize a passage word line at this time, the first gate electrode including the usual side attachment wall is formed by the Pori Si layer, and its structure connected with second another gate electrode is [ the first gate electrode and passage word line ] desirable. It is more desirable to embed the first gate inter-electrode by the insulator layer, and to make it form furthermore. Although the example which forms a capacitor on a bit line was described here, a bit line may be constituted on a capacitor and a capacitor may be formed after wiring. By doing in this way, the MOSFET structure using a fence is applicable to the transistor of the stack mold capacitor DRAM.

[0283] (The 22nd operation gestalt) A \*\*\*\* 22 operation gestalt is related with the structure of the gate electrode in the case of arranging two or more (this example showing two cases) MOSFET components with a fence.

[0284] The perspective view showing MOSFET which drawing 58 requires for the 22nd operation gestalt of this invention, the sectional view where that top view and drawing 59 B meet a 59in drawing 59 A B-59B line in drawing 59 A, the sectional view where drawing 59 C meets the 59C-59C line in drawing 59 A, and drawing 59 D are the sectional views in alignment with the 59D-59 D line in drawing 59 A. In addition, in drawing 58 and drawing 59 A - drawing 59 D, the contact shown, for example in drawing 2 A of the 1st operation gestalt, wiring, and a side-attachment-wall insulator layer are omitted, respectively.

[0285] As shown in drawing 58 and drawing 59 A - drawing 59 D, arrangement, fence 13 [ for example, ], arranges two or more fences 13 by the minimum design rule mutually to high density.

[0286] In this case, the polycrystal Si layer which is 1st gate electrode 16a is completely embedded among fence 13, and the metal film (for example, W film, aluminum film, TiN film) and silicide film (for example, TiSi2 film, WSi2 film, CoSi2 film, etc.) which are 2nd gate electrode 16b serve as structure formed on the front face of 1st gate electrode 16a which became flat.

[0287] Thus, by forming 2nd gate electrode 16b on the front face of 1st gate electrode 16a which became flat, formation of the metal film which is the ingredient of for example, 2nd gate electrode 16b, or the silicide film becomes easy, or an advantage, like processing of a gate electrode becomes easy can be acquired.

[0288] Since the front face of 2nd gate electrode 16b can furthermore also be made flat, after processing of a gate electrode can acquire the advantage that the same production process as the conventional flat-surface mold MOSFET can be used.

[0289] (The 23rd operation gestalt) A \*\*\*\* 23 operation gestalt is related with the structure of the gate electrode in the case of arranging two or more (this example showing two cases) MOSFET components with a fence like the 22nd operation gestalt.

[0290] The perspective view and drawing 61 which show MOSFET which drawing 60 requires for the 23rd operation gestalt of this invention are that sectional view. In addition, the cross section of drawing 60 is equivalent to the cross section shown in drawing 59 B. Moreover, in drawing 60 and drawing 61, the contact shown, for example in drawing 2 A of the 1st operation gestalt, wiring, and a side-attachment-wall insulator layer are omitted, respectively.

[0291] As shown in drawing 60, the polycrystal Si layer which is 1st gate electrode 16a is made thin to about 20nm. And it is also possible to embed the metal film which is 2nd gate electrode 16b, and the silicide film among 1st gate electrode 16a.

[0292] With such a 23rd operation gestalt, the front face of 2nd gate electrode 16b can be made flat, for example, and after processing of a gate electrode can acquire the advantage that the same production process as the conventional flat-surface mold MOSFET can be used.

[0293] (The 24th operation gestalt) The perspective view showing the contact section of MOSFET which drawing 62 requires for this invention, the top view showing the contact section of MOSFET which drawing 63 A requires for this invention, the side elevation seen from the direction of the arrow head B which shows drawing 63 B to drawing 63 A, and drawing 63 C are the side elevations seen from the direction of the arrow head C shown in drawing 63 A. In addition, in drawing 62 and drawing 63 A - drawing 63 C, the contact shown, for example in drawing 2 A of the 1st

operation gestalt, wiring, and a side-attachment-wall insulator layer are omitted, respectively.

[0294] As shown in drawing 62 and drawing 63 A - drawing 63 C, in MOSFET concerning this invention, the parts (below electric-contact section) 50 of the source / drain field 17 to which the contact plug 28 is connected are straddling fundamentally a part of top faces (TOP) of a fence 13, and its two side faces (SIDE I, SIDE II) in which it faces mutually, respectively.

[0295] This structure is structure in which that thing [ going caudad and extending ] is possible along the side face of a fence 13 about the electric contact section 50. For this reason, even if it does not expand the width of face of a fence 13 on the width of face of the source / drain field 17, and a concrete target, area of the electric contact section 50 can be enlarged, for example, the advantage of the contact plug 28, and the source / drain field 17 that the increment in contact resistance can be controlled can be acquired.

[0296] A \*\*\*\* 24 operation gestalt tends to offer further reducible structure for the flat-surface area of MOSFET, without spoiling the above-mentioned advantage.

[0297] The perspective view showing MOSFET which drawing 64 requires for the 24th operation gestalt of this invention, the side elevation which saw from the direction of the arrow head B with which drawing 65 A shows that top view and drawing 65 B to drawing 65 A, and drawing 65 C are the side elevations seen from the direction of the arrow head C shown in drawing 65 A.

[0298] As shown in drawing 64 and drawing 65 A - drawing 65 C, in addition to a part of top faces (TOP) of a fence 13, and its two side faces (SIDE I, SIDE II) in which it faces mutually, in MOSFET concerning a \*\*\*\* 24 operation gestalt, the electric contact section 50 is straddling a part of other two side faces (SIDE III, SIDE IV) adjacent to each of these two side faces (SIDE I, SIDE II).

[0299] This structure is also the structure in which that thing [ going caudad and extending ] is possible along the side face of a fence 13 about the electric contact section 50. further -- a \*\*\*\* 24 operation gestalt -- the electric contact section 50 -- a part of other two side faces (SIDE III, SIDE IV) -- \*\*\*\*\* -- the die length of a fence 13, for example, the die length which met in the direction of channel length, can be shortened by things, controlling the area fall of the electric contact section 50.

[0300] Therefore, it is possible to reduce the flat-surface area of MOSFET further, without spoiling the advantage explained with reference to drawing 62 and drawing 63 A - drawing 63 C.

[0301] (The 25th operation gestalt) A \*\*\*\* 25 operation gestalt is related with the structure which can ease gate electric-field concentration.

[0302] Drawing 66 is the sectional view showing MOSFET concerning the 25th operation gestalt of this invention. In addition, the cross section shown in drawing 66 is equivalent to the cross section shown in drawing 2 B of the 1st operation gestalt.

[0303] For example, with the 2nd operation gestalt, gate-dielectric-film 18b formed in the top face of a fence 13 is made thicker than gate-dielectric-film 18a formed in the side face of a fence 13. It explained that fluctuation of the threshold electrical potential difference which could ease the gate electric-field concentration in the up corner of the channel field 15, and originated in gate electric-field concentration by this, and fluctuation of a substrate bias property could be controlled.

[0304] In MOSFET concerning a \*\*\*\* 25 operation gestalt, as shown in drawing 66, contrary to the 2nd operation gestalt, gate-dielectric-film 18b formed in the top face of a fence 13 is made thinner than gate-dielectric-film 18a formed in the side face of a fence 13.

[0305] Such structure can acquire the side face of a fence 13 in the process explained with reference to drawing 7 A of the 1st operation gestalt, and drawing 7 B by oxidizing so that it may become thicker than the insulator layer formed in the top face.

[0306] With this structure, when the up corner shown in drawing 66 and in a broken-line circle serves as a round configuration, the gate electric-field concentration in an up corner can be eased, and it becomes possible to control fluctuation of the threshold electrical potential difference resulting from gate electric-field concentration, and fluctuation of a substrate bias property like the 2nd operation gestalt.

[0307] (The 26th operation gestalt) A \*\*\*\* 26 operation gestalt is related with the structure which can ease gate electric-field concentration as well as the 25th operation gestalt.

[0308] Drawing 67 is the sectional view showing MOSFET concerning the 26th operation gestalt of this invention. In addition, the cross section shown in drawing 67 is equivalent to the cross section shown in drawing 2 B of the 1st operation gestalt.

[0309] As shown in drawing 67, the place where a \*\*\*\* 26 operation gestalt differs from the 25th operation gestalt is having formed gate-dielectric-film 18a formed in the side face of a fence 13 by deposition of an insulating material.

[0310] After the process explained with reference to drawing 6 A of the 1st operation gestalt, and drawing 6 B, on the whole surface, deposition formation of the high dielectric film can be carried out preferably, a high dielectric film can be etched after this using the RIE method, and such structure can be acquired by the insulator layer and leaving the side face of a fence 13.

[0311] Also in this structure, when the up corner show in drawing 67 and in a broken line circle be make to a round configuration, the gate electric field concentration in an up corner can be ease, and it become possible to control fluctuation of the threshold electrical potential difference resulting from gate electric field concentration, and fluctuation of a substrate bias property like the 2nd operation gestalt.

[0312] (The 27th operation gestalt) Perspective view and drawing 68 B which shows MOSFET which drawing 68 A requires for the 27th operation gestalt of this invention is that side elevation.

[0313] As shown in drawing 68 A and drawing 68 B, the gate electrode 16 of MOSFET concerning the 27th operation gestalt has side-attachment-wall gate section 16a and top-face gate section 16b, and is constituted. Side-attachment-wall gate section 16a is formed on gate-dielectric-film 18a formed on the side face of a fence 13. Moreover, top-face gate section 16b is formed on gate-dielectric-film 18b (omitted in drawing 68 A and drawing 69 B) formed on the top face of a fence 13. And the gate length L1 of side-attachment-wall gate section 16a is shorter than the gate length L2 of top-face gate section 16b.

[0314] Next, an example of the manufacture approach of MOSFET concerning the 27th operation gestalt is explained using drawing 78 from drawing 69. In addition, sectional view [ where top view and drawing 69 B - drawing 78 B meets the B-B line in drawing 69 A - drawing 78 A, respectively in drawing 69 A - drawing 78 A ], drawing 69 C - drawing 78 C is a sectional view which meets the C-C line in drawing 69 A - drawing 78 A, respectively.

[0315] First, as shown in drawing 69 A - drawing 69 C, sequential formation of the mask layer (SiN) 21 which has the thickness of about 20,100nm of SiO two-layer which has about 5nm thickness on the front face of the P type Si substrate 10 by the process explained with the 1st operation gestalt and the same process, and the mask layer (SiO<sub>2</sub>) 22 with about 100nm thickness is carried out. Then, while etching about 150nm and forming a slot, the fence 13 with width of face of about 100nm is formed for the P type Si substrate 10.

[0316] Next, as shown in drawing 70 A - drawing 70 C, Mizouchi formed in the Si substrate 10 is filled up with an insulating material (SiO<sub>2</sub>) 23 by the process explained with the 1st operation gestalt, and the same process. Thereby, shallow trench isolation is formed in the Si substrate 10. In this example, it leaves the mask layer (SiN) 21 on a fence 13.

[0317] Next, as shown in drawing 71 A - drawing 71 C, on the structure shown in drawing 70 A - drawing 70 C, a photoresist is applied and the photoresist film 50 is formed. Subsequently, the aperture 51 corresponding to a side-attachment-wall gate section formation pattern is formed in the photoresist film 50 using the lithography method. In this example, it is exposed of the part corresponding to the side-attachment-wall gate section formation field of an insulating material (SiO<sub>2</sub>) 23, and the mask layer (SiN) 21 from an aperture 51, respectively.

[0318] Next, as shown in drawing 72 A - drawing 72 C, the photoresist film 50 and the mask layer (SiN) 21 are used for a mask, respectively, and about 100nm (SiO<sub>2</sub>) of insulating materials 23 is etched from the interface of SiO two-layer 20 as a fence 13. Thereby, the slot 52 with a depth of about 100nm and width of face of about 100nm for side-attachment-wall gate section embedding is formed in an insulating material (SiO<sub>2</sub>) 23.

[0319] Next, as shown in drawing 73 A - drawing 73 C, the photoresist film 50 is removed. Subsequently, gate-dielectric-film 18a which consists of SiO<sub>2</sub> is formed on the side face of the fence 13 exposed from the slot 52.

[0320] Next, as shown in drawing 74 A - drawing 74 C, the doped polycrystal Si film 53 with which the N type impurity was doped is formed on the structure shown in drawing 73 A - drawing 73 C. Thereby, a slot 52 is embedded with the doped polycrystal Si film 53, and side-attachment-wall gate section 16b is formed among the gate electrodes 16. Subsequently, the metal film 54 is formed on the doped polycrystal Si film 53. W film can be mentioned as an example of the metal film 54.

[0321] Next, as shown in drawing 75 A - drawing 75 C, the resist film (not shown) is used for a mask and the metal film 54, the doped polycrystal Si film 53, the mask layer (SiN) 21, and SiO two-layer 20 are etched. Thereby, while top-face gate section 16b is formed among the gate electrodes 16, the top face of a fence 13 is exposed. The top face of a fence 13 is equivalent to the flat-surface pattern of the active area of MOSFET. In this example, the gate length L2 of top-face gate section 16b is set up for a long time than the gate length L1 of side-attachment-wall gate section 16a. Gate length L1 is [ about 140nm and the gate length L2 of an example of the numeric value ] about 100nm.

[0322] Next, as shown in drawing 76 A - drawing 76 C, top-face gate section 16b and an insulating material 23 are used for a mask, and the ion implantation of N type impurity ion, for example, the phosphorus ion, is carried out into a fence 13. This forms N-mold diffusion layer 17a in a fence 13. In addition, this N-mold diffusion layer 17a functions as



for example, an extension layer, and is formed if needed. Therefore, omitting is also possible.

[0323] Next, as shown in drawing 77 A - drawing 77 C, on the structure shown in drawing 76 A - drawing 76 C, a CVD method is used and an insulating material, for example, SiO<sub>2</sub> and SiN, is deposited. Subsequently, RIE of the deposited insulating material is carried out, and it leaves this insulating material on the side attachment wall of the gate electrode 16. Thereby, the side-attachment-wall insulator layer 25 is formed. Moreover, in this example, as shown in drawing 75 A - drawing 75 C, the step has arisen between the insulating material 23 and the top face of a fence 13 by having removed the mask layer (SiN) 21 from on the top face of a fence 13. For this reason, the above-mentioned insulating material remains also on the side attachment wall of an insulating material 23. Thereby, the side-attachment-wall insulator layer 25 is formed also on the side attachment wall of an insulating material 23.

[0324] Next, as shown in drawing 78 A - drawing 78 C, top-face gate section 16b, an insulating material 23, and the side-attachment-wall insulator layer 25 are used for a mask, and the ion implantation of N type impurity ion, for example, the arsenic ion, is carried out into a fence 13. This forms N<sup>+</sup> mold diffusion layer 17 in a fence 13. N<sup>+</sup> mold diffusion layer 17 functions as the source / a drain field of NMOS. Subsequently, an interlayer insulation film 26 is formed on top-face gate section 16b, N<sup>+</sup> mold diffusion layer 17, an insulating material 23, and the side-attachment-wall insulator layer 25. Subsequently, N<sup>+</sup> mold diffusion layer 17 and the contact hole 27 which reaches up gate section 16b are formed in an interlayer insulation film 25. Subsequently, it is filled up with electric conduction objects, such as tungsten film, in a contact hole 27, and the contact plug 28 is formed. Subsequently, the wiring layer 29 which contacts the contact plug 28 electrically is formed on an interlayer insulation film 26.

[0325] Thus, MOSFET concerning the 27th operation gestalt can be formed.

[0326] According to the MOSFET concerning such a 27th operation gestalt, in addition to the effectiveness acquired from the operation gestalt mentioned above, the following effectiveness can be acquired further.

[0327] (1) Make gate length L1 of side-attachment-wall gate section 16a shorter than the gate length L2 of top-face gate section 16b. Thereby, the effectual gate length of MOSFET becomes shorter than the gate length L1 of top-face gate section 16b. For this reason, that engine performance increases compared with the planar mold MOSFET with the same flat-surface pattern as MOSFET concerning the 27th operation gestalt. For example, the speed of response of MOSFET improves because effectual gate length becomes short. Of course, since channel width also increases by having side-attachment-wall gate section 16b compared with the planar mold MOSFET with the same flat-surface pattern, current drive capacity also becomes large, for example.

[0328] (2) The channel length L1 of top-face gate section 16b can be long, namely, can enlarge the cross section as gate wiring. If the cross section of gate wiring becomes large, the resistance of gate wiring will become small. If the resistance of gate wiring becomes small, the situation of the signal delay in gate wiring will also be eased, and the engine performance as an integrated circuit will also increase.

[0329] (3) Moreover, according to that manufacture approach, form the slot 52 for side-attachment-wall gate section embedding in an insulating material 23, and fill it up with the electric conduction object which becomes side-attachment-wall gate section 16a in this slot 52. Compared with the case where patterning of the electric conduction object used as the gate electrode 16 is carried out ranging over a fence 13, it is easy to manufacture such a manufacture approach.

[0330] (4) The process which furthermore fills up a slot 52 with the electric conduction object used as side-attachment-wall gate section 16a can apply the present shallow trench technique etc. And after filling up a slot 52 with the electric conduction object used as side-attachment-wall gate section 16a, it can form in it using the manufacturing technology of the usual planar mold MOSFET. The manufacture approach introduced with the 27th operation gestalt from these viewpoints can form MOSFET which starts this invention using a current manufacturing technology, and is high. [ of practicality ]

[0331] In addition, such a manufacture approach is not used only within the case where MOSFET concerning the 27th operation gestalt is manufactured, and also when manufacturing MOSFET concerning the 1st - the 27th operation gestalt, it can be used.

[0332] As mentioned above, according to this invention explained according to the 1st - the 27th operation gestalt, between the isolation insulator layers formed in the source / drain field formed into (1) fence, and the lower field of a fence is detached.

[0333] MOSFET with various channel width is accumulable into 1 chip, being able to control the channel width of MOSFET by the depth of the source / drain field, and controlling the increment in flat-surface area according to this configuration.

[0334] (2) Make width of face (Wg) of a fence narrower than 0.20 micrometers.

[0335] According to this configuration, a channel field depletion-izes completely with the gate electrode formed in the

side face of a fence. When a channel field depletion-izes completely, it becomes possible to low-concentration-ize high impurity concentration of a channel field compared with the high impurity concentration of the channel field of the flat-surface mold MOSFET. And by low-concentration-izing high impurity concentration of a channel field, and it is [ which can control the fall of the carrier mobility in a channel field ] hard to be influenced of fluctuation by high impurity concentration, strong structure is realizable to the thickness variation of gate dielectric film.

[0336] (3) Make a part of [ at least ] thickness of the gate dielectric film between the top face of a fence, and a gate electrode thicker than the thickness of the gate dielectric film between the side face of a fence, and a gate electrode, or make it thin.

[0337] According to this configuration, the gate electric-field concentration in the up corner of a fence can be eased, and control of a threshold electrical potential difference becomes easy.

[0338] (4) Prepare a high concentration impurity layer between the channel field of a fence, and a well or a substrate.

[0339] According to this configuration, the punch-through of MOSFET can be prevented.

[0340] (5) In the side face of a fence, make the source, a drain, and distance of a between large as it is short in an up field and becomes the lower part.

[0341] According to this configuration, the punch-through of MOSFET can be prevented.

[0342] (6) Make the source / drain field, and the gate electrode of each other offset in the side face of a fence.

[0343] According to this configuration, the punch-through of MOSFET can be prevented.

[0344] (7) Prepare two or more fences and form a gate electrode in these side faces in common.

[0345] According to this configuration, bigger channel width is realizable in little flat-surface area.

[0346] (8) Prepare the convex thin film Si layer for gate contact besides a fence.

[0347] According to this configuration, the depth of a contact hole can be mostly arranged with the source / drain field, and each gate electrode, and the manufacture yield can be improved.

[0348] (9) When forming contact in the source / drain field of a fence, form in a part of side face at least not only in the top face of a fence.

[0349] According to this configuration, contact resistance can be reduced, without spoiling the increment in flat-surface area.

[0350] (10) It is not almost perpendicular, for example, make the inclination (cone angle) of the side face of a fence into the forward tapered shape of about 85 degrees.

[0351] According to this configuration, processing of the gate electrode in the side face of a convex thin film Si layer can be made easy.

[0352] (11) Form the gate electrode formed along the side face of a fence for example, by the polycrystal Si film, and connect the 2nd gate electrode which turns into this gate electrode from for example, the metal film or the silicide film.

[0353] According to this configuration, the height of the gate electrode which both adjoins as if resistance of a gate electrode can be reduced can be made low. Therefore, while accommodation of the gate electrode characteristic is attained, gate inter-electrode parasitic capacitance can be reduced.

[0354] (12) Form the gate dielectric film of a fence formed on a side face at least by high dielectric insulator layers, such as for example, 2OTa5 film.

[0355] According to this configuration, the capacity between a gate electrode and a channel field can be increased, and the cut-off characteristic of MOSFET can be improved more effectively.

[0356] (13) Consider as the round configuration of a fence which makes the include angle of the up corner of a channel field about 45 degrees from a perpendicular mostly, or can approximate it by the semicircle with a radius of about 30nm at least.

[0357] According to this configuration, the gate electric-field concentration in the up corner of a fence can be eased, and control of a threshold electrical potential difference becomes easy.

[0358] (14) Make into the structure including LDD high concentration source / drain field, and low-concentration low-concentration source / drain field instead of the single source / drain structure the source / drain field formed in the fence.

[0359] According to this configuration, the electric field the source / near the drain field can be eased, and the dependability of a transistor can be improved.

[0360] (15) While preparing two or more fences and forming a gate electrode in these side faces in common, combine mutually a part of field of two or more fences which includes the source / drain field at least.

[0361] According to this configuration, while bigger channel width is realizable in little flat-surface area, the number of the contacts to the source / drain field is reducible.

[0362] (16) Prepare the impurity layer of a different conductivity-type mold from the source / drain field between the

pars basilaris ossis occipitalis of the source / drain field formed in the fence, and the insulator layer formed in the bottom of a fence.

[0363] According to this configuration, when a fence is formed, for example on a SOI substrate, the variation in the thickness of a SOI layer can be absorbed to the variation in the depth of the source / drain field.

[0364] (17) When a fence is formed using the amorphous silicon formed on the glass substrate, the effectiveness mentioned above can be acquired by adopting the configuration of above-mentioned (1) - (16).

[0365] (18) A fence forms a slot and forms it into this slot in the epitaxial Si layer which carried out epitaxial growth.

[0366] According to this configuration, it is stabilized, the isolation insulator layer formed around a fence can be formed, and the manufacture yield of semiconductor integrated circuit equipment can be improved.

[0367] (19) When forming a CMOS circuit by NMOSFET formed in the fence, and PMOSFET formed in other fences, change mutually the depth of the P type source / drain field, and the depth of the N type source / drain field.

Specifically, the depth of the P type source / drain field is made deeper than the depth of the N type source / drain field.

[0368] According to this configuration, the difference of the superficial design dimension of NMOSFET and PMOSFET resulting from the difference of electronic mobility and the mobility of an electron hole can be contracted. When especially a CMOS circuit is designed, the area of PMOSFET can be reduced and the whole circuit area can be reduced.

[0369] (20) When forming a MOS circuit by NMOSFET (or PMOSFET) formed in the fence, and NMOSFET (or PMOSFET) formed in other fences, change mutually the depth of the source / drain field of these NMOSFET(s) (or PMOSFET).

[0370] When according to this configuration a superficial design dimension can realize the same NMOSFET (or PMOSFET) from which channel width differed mutually but and designs a circuit, channel width can reduce the area of large NMOSFET (or PMOSFET), and can reduce the whole circuit area.

[0371] as mentioned above, although the 1st - the 27th operation gestalt explained this invention, it is not limited to each of these operation gestalt, and in that operation, in the range which does not deviate from the summary of invention, many things are boiled and this invention can be deformed

[0372] For example, it is possible to also make the flat-surface mold MOSFET coexist with MOSFET concerning this invention on the same Si wafer substrate. In this case, what is necessary is just to employ the features of MOSFET concerning this invention, and the features of the flat-surface mold MOSFET efficiently, respectively.

[0373] Moreover, although the operation gestalt mainly explained the MOSFET component of a simple substance, it is applicable to a flash memory, SRAM and DRAM, various logical circuits, CPU, etc. using this MOSFET. This component structure can control the short channel effect, and is effective in detailed-izing of a P channel and N-channel metal oxide semiconductor FET, The cut-off characteristic of a component improves by perfect depletion-ization of a channel, The current drive capacity of MOSFET improves according to double-gate structure, The channel width of an N channel and a P channel by that it can realize by adjustment of the depth of the source / drain field, without increasing flat-surface design area, and dividing into convex [ two or more / Si ] Taking advantage of the features, like the MOSFET component of a high current is realizable in a small area, it is applicable as new MOSFET component structure which transposes the conventional flat-surface mold MOSFET component to an LSI circuit at large.

[0374] Moreover, it combines suitably and, of course, each above-mentioned operation gestalt can also be carried [ independence or ] out.

[0375] Furthermore, invention of various phases is included in each above-mentioned operation gestalt, and it is also possible to extract invention of various phases with a proper combination of two or more requirements for a configuration indicated in each operation gestalt.

[0376]

[Effect of the Invention] As explained above, according to this invention, the semiconductor device with the structure which can attain high performance-ization using a part of side face of a convex semi-conductor layer, and its manufacture approach can be offered as a channel field at least.

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[Translation done.]